Embedded Boundary-Scan Testing

1st International Board Test Workshop

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Bell Labs Innovations

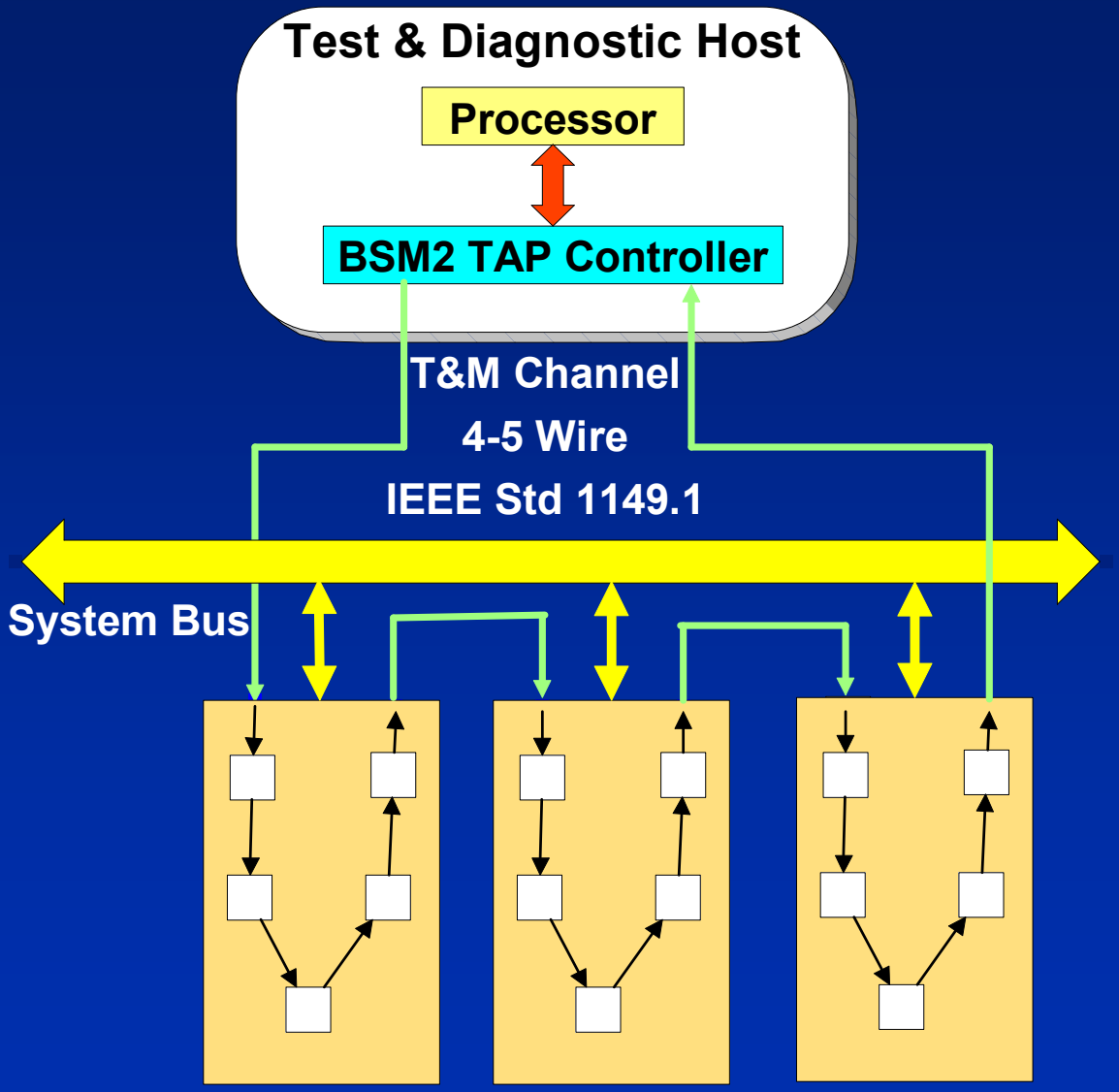
Purpose

- Embedded tests are typically functional tests that are expensive to create
- Boundary-Scan tests
  - Structural: allowing automatic generation
  - Explicit coverage metrics
  - Vector based
- Embedded Boundary-Scan provides Built-In Test/Test Anywhere capability

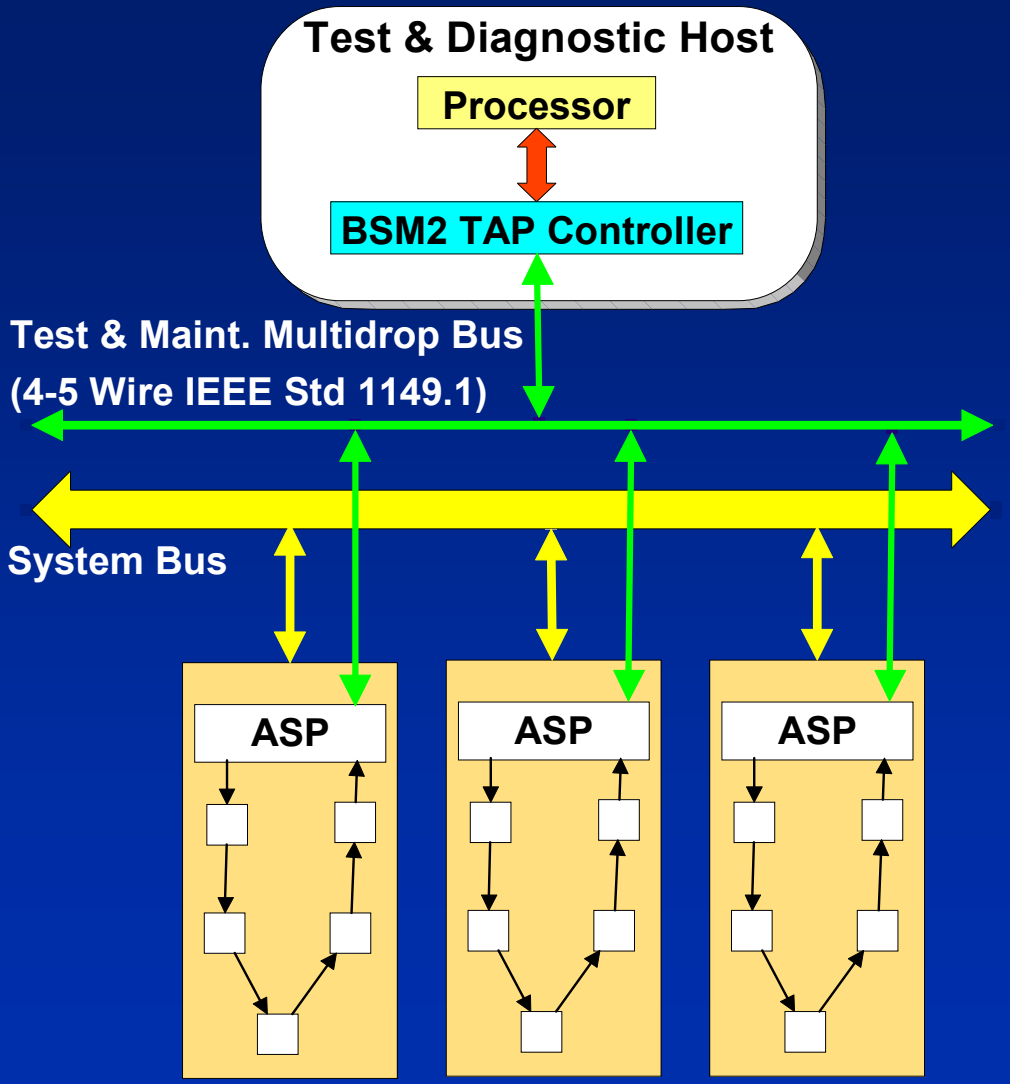
Outline

- System Test Architectures
- Embedded Test Software
- Embedded Test Generation Process
- Case Studies
- Benefits
- Traps and Pitfalls

Serial Scan Chain Architecture



Multidrop Scan Chain Architecture



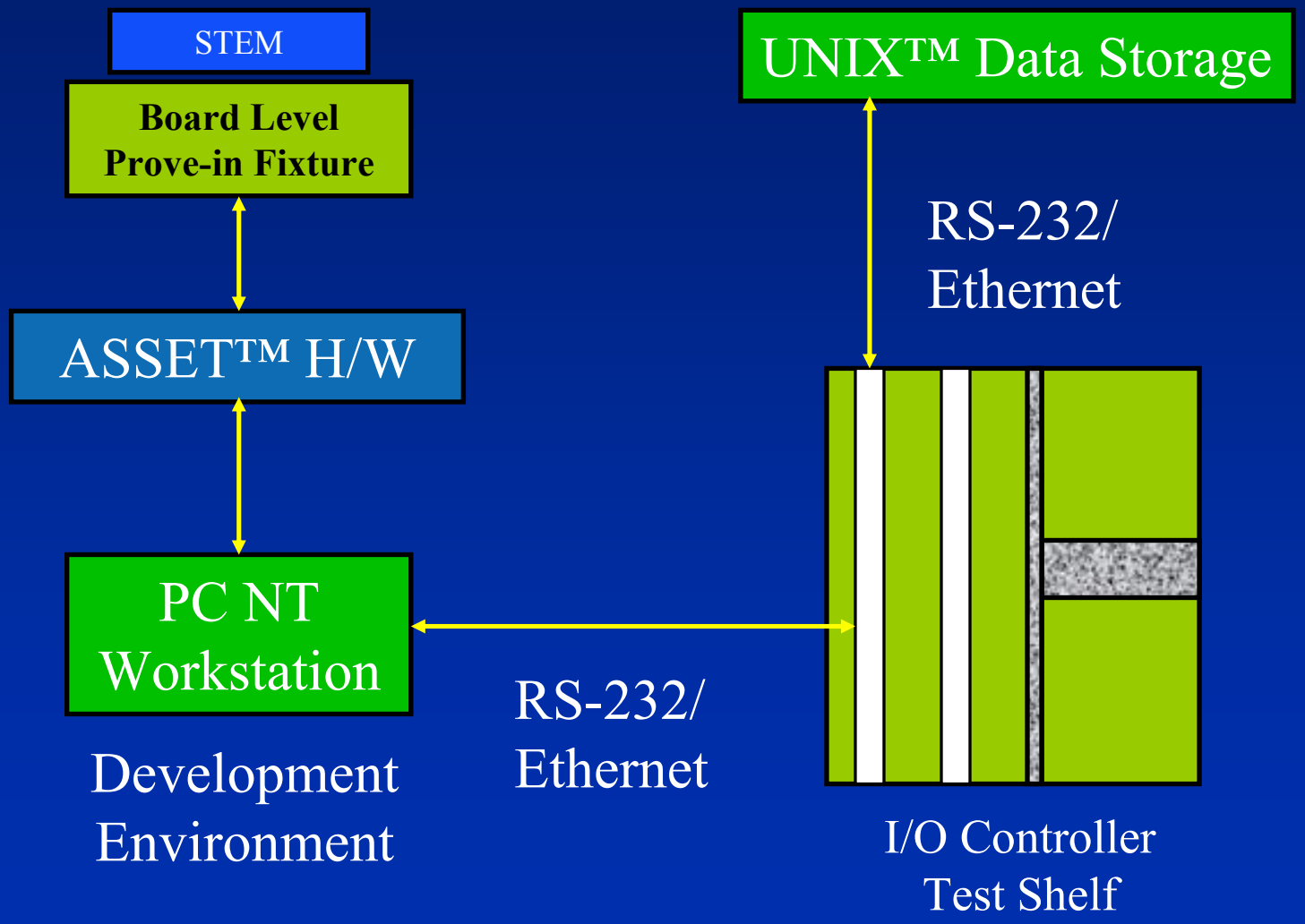
Embedded Test Software

- API for Boundary-Scan Test application
- Test Flow Control Language™ (TFCL)
- Decoupled/Independent from test data
- Modular & Persistent Test Steps
  - ASP Selection
  - SVF Application
  - STAPL Application
- C++ code

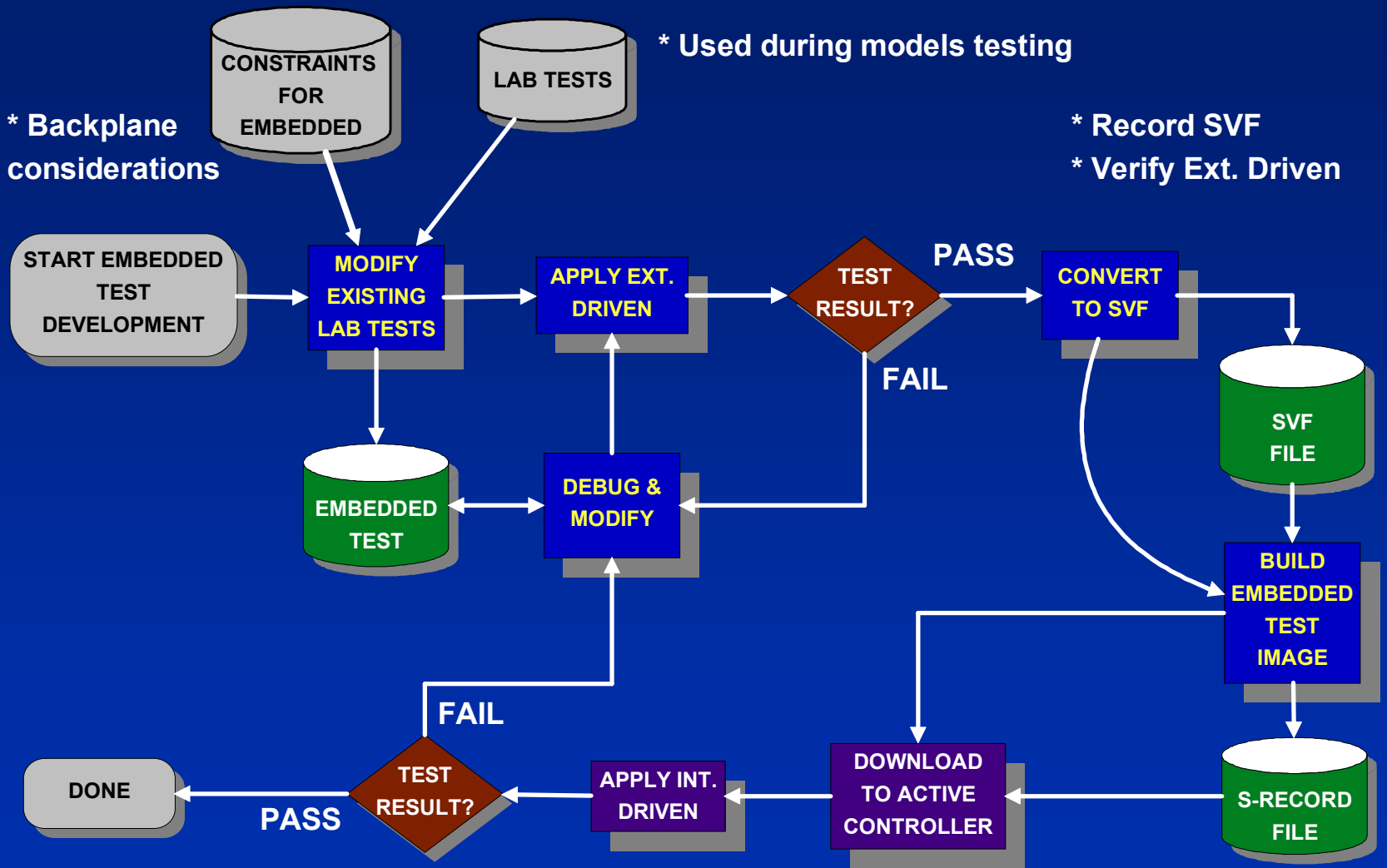
TFCL Example

```
ENTITY sys
FLOW sys IS
APPLY ASP FROM 0x1 TO 0x1 DIAGNOSE;
IF NOT FAIL THEN
   APPLY inter1 DIAGNOSE LINE PIN NET;
   IF FAIL THEN
        PRINT("Interconnect test failed!");
   ELSE
        PRINT("All tests passed!");
   END IF;
ELSE
   PRINT("Unable to connect to board!");
END IF;
END FLOW;
END ENTITY;
```

Embedded Test Station

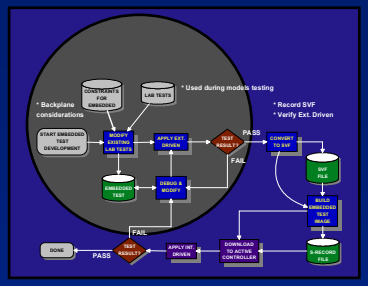


Embedded Test Generation Process



Embedded Test Generation Process

Embedded Vector Generation



* Backplane considerations

CONSTRAINTS FOR EMBEDDED

LAB TESTS

* Used during models testing

START EMBEDDED TEST DEVELOPMENT

MODIFY EXISTING LAB TESTS

APPLY EXT. DRIVEN

TEST RESULT?

PASS

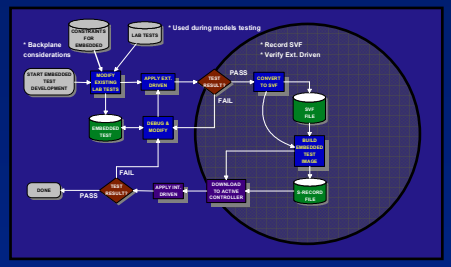
FAIL

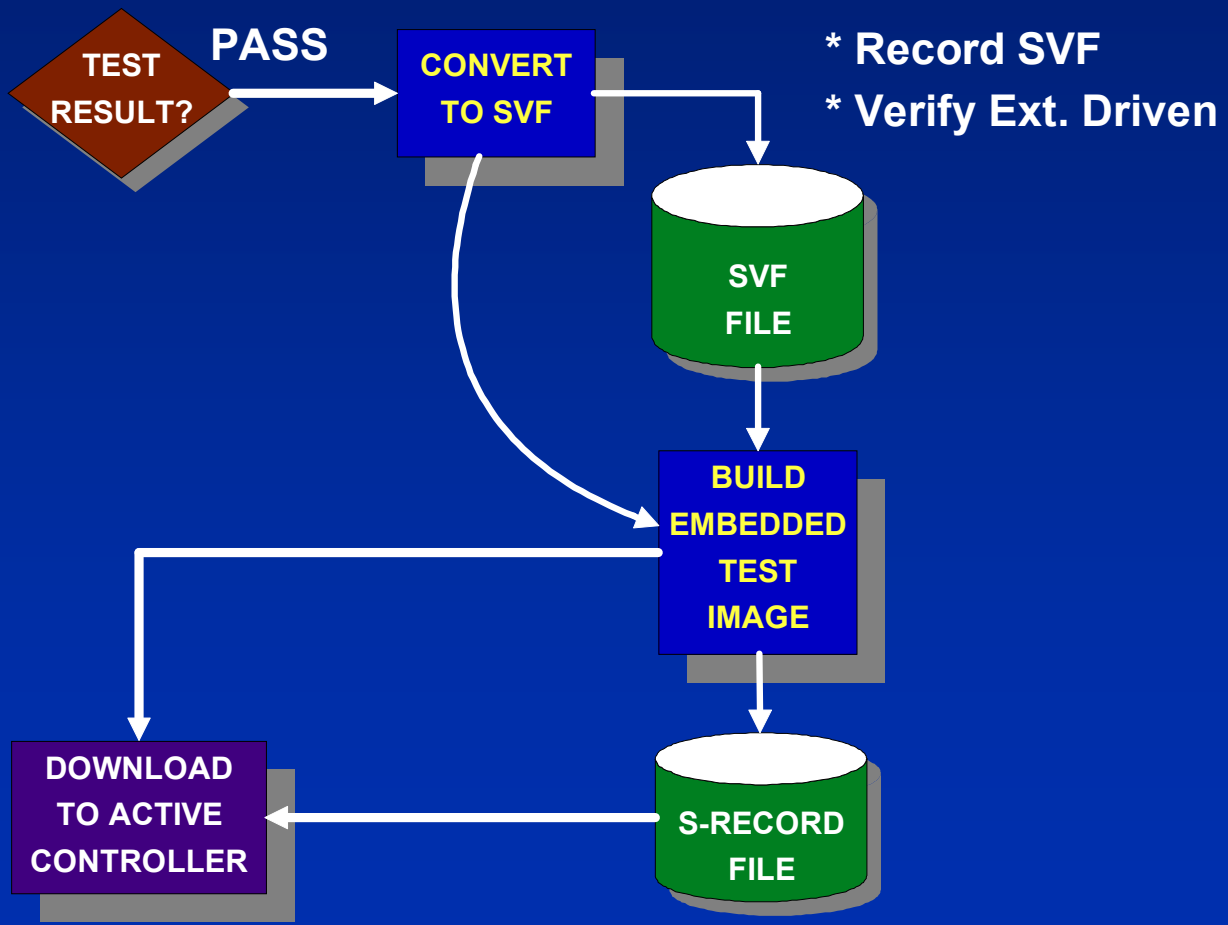
EMBEDDED TEST

DEBUG & MODIFY

Embedded Test Generation Process

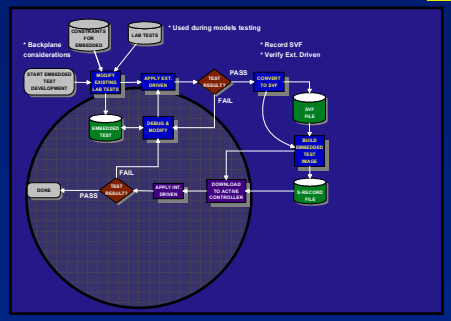
Embedded Vector Porting

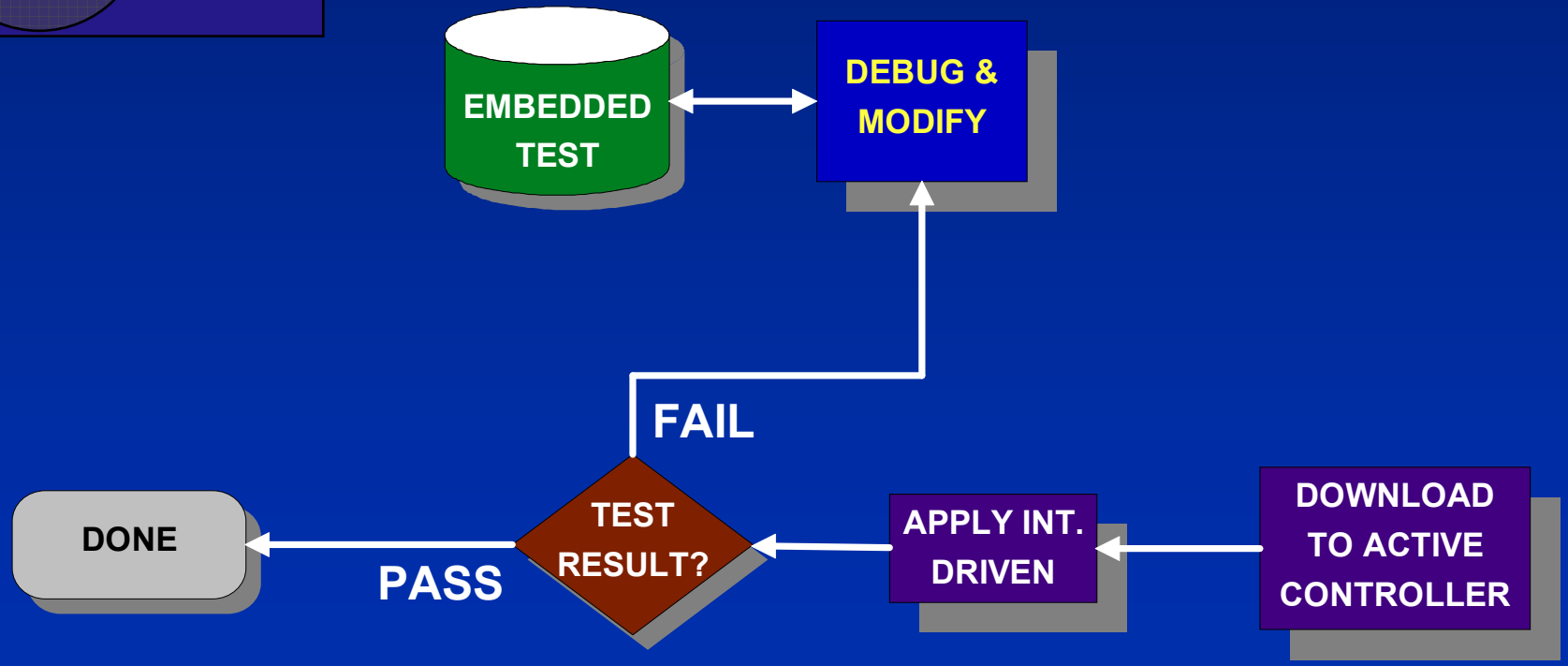




Embedded Test Generation Process

Embedded Test Application





Duplex Test Case Study

- 2431 nets, 29 Bscan devices, ~70 non-Bscan devices
- 51.3% coverage by ATPG tools
- Test Vectors Stored in UUT FLASH
- Standalone program resident in FLASH
- Used by H/W Lab, S/W Lab, EST, Mfg. Func. Test

Simplex Test Case Study

- Dual design board
- Controller tests feature half
- Test Vectors downloaded via Ethernet
- Level 2 boot version of program
- OA&M version of program for off-line testing
- Remote test provision

Benefits

- Enhanced coverage at functional test
- No setup – In-line testing realized
- Tests usable anywhere
- Failure diagnostics available, but limited
- Test Data may reside with UUT
- Test coverage different over life cycle

Benefits (Continued)

- Remote field upgrades possible
- Migrated to EST Chamber testing
- Our environment allowed for data compression of the test vectors (~70% compression)
- Factory testing of vectors validates tests for use as periodic field tests

Traps and Pitfalls

- Fault recovery
- UUT recovery
- Isolated control H/W architecture
- Test data management/versioning
- Chain configuration management

Conclusion

- Natural extension to external testing
  - Many additional constraints/issues
- Built-in Test – Test Anywhere
- Program and data decoupling
- Flexible environment using TFCL
- Needs friendly H/W architecture

Conclusion (Continued)

- Test reuse/salvage amortizes development cost
- Reduces functional test development
- Location of test data can influence data management cost