

# JTAG System Test in a MicroTCA World



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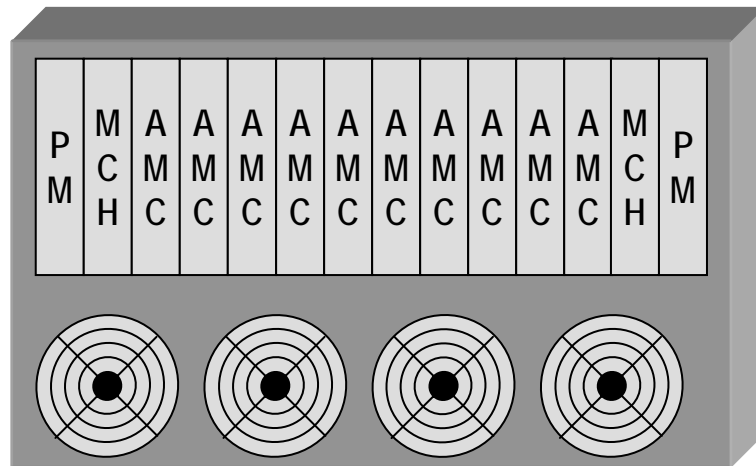


# Outline

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- 50,000 ft Overview of MicroTCA
- Decision Process for System-Level JTAG Architecture
- Overview of the JTAG Switch Module
- Programming and Chain Selection Issues
- Conclusions

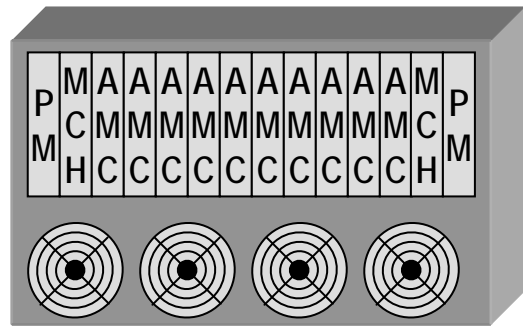
# 50,000 ft Overview of MicroTCA



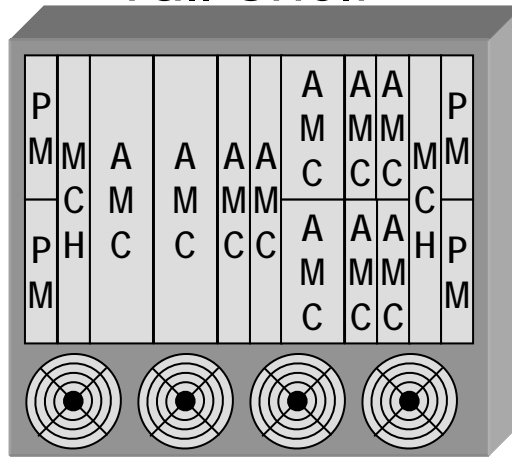
- Complimentary standard to PICMG 3.0 (ATCA)
- Designed to address cost sensitive and physically smaller applications
- Deploys Advanced Mezzanine Cards (AMCs) as blades facilitating collections of high diversity and high density
- Virtualizes the ATCA Carrier
  - AMCs plug directly into a stand-alone chassis backplane
  - MicroTCA Carrier Hub (MCH) modules provide fabric interconnection and system management functions
- Standardized Power Management
- Dynamically configurable/ supports Hot Swap
  - AMCs already support JTAG at edge
  - MicroTCA Goal: MUST support System-Level JTAG Test

# MicroTCA Packaging Options

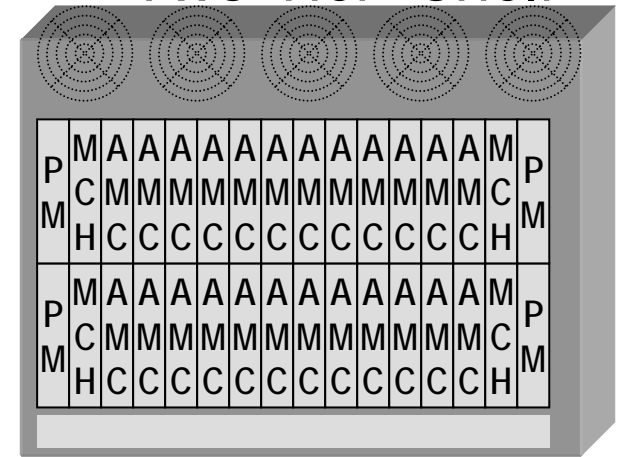
## Single Shelf



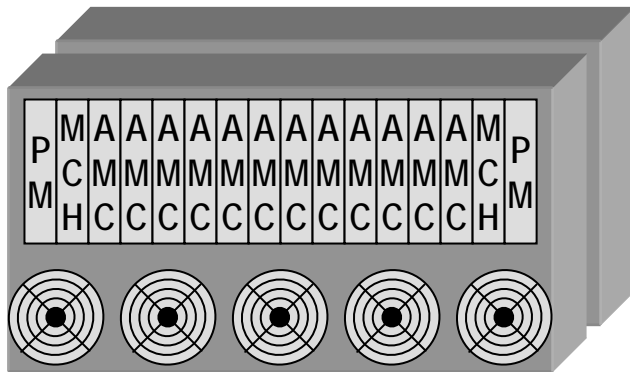
## Tall Shelf



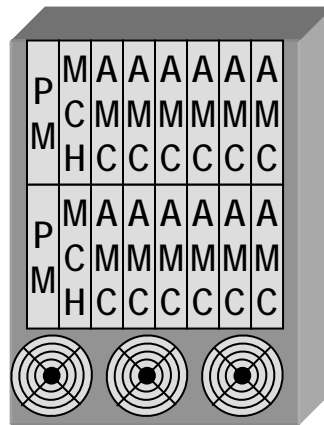
## Two Tier Shelf



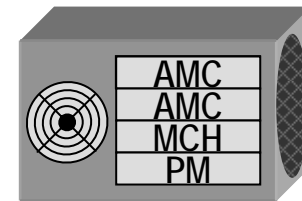
## Back-to-Back Shelf



## Cube Shelf



## Pico Shelf



# Decision Process for System-Level JTAG Architecture

## *Pipe Dreams*

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- First industry standard system bus architecture to be designed to support JTAG testing at the system level
- AMC standard already supports JTAG at edge
- Need **test architecture as flexible as Multi-drop** but does not require gateway devices to apply JTAG tests/upgrades to each AMC from external and embedded testers
- What test structure should be used?
  - Ring/Daisy-chained TAP
  - Full Star/Radial Interface
  - Multi-drop
  - JTAG over IPMI/IPMB
  - JTAG over Ethernet

# Decision Process for System-Level JTAG Architecture

## *Problems Encountered*

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- Ring/Daisy-chained TAP
  - Chain modified if slot depopulated or upgraded
- Full Star/Radial Interface
  - Not enough pins available on MicroTCA Carrier Hub (MCH)
- Multi-drop
  - No gateway devices on AMCs
- JTAG over IPMI/IPMB
  - New IPMI protocols needed
  - Performance of current IPMB in MicroTCA not fast enough
  - Change required for AMC and IPMI specifications
- JTAG over Ethernet
  - New protocols needed
  - Requires AMC to be programmed and partially working
  - Change required for AMC specification

# Decision Process for System-Level JTAG Architecture

## *Agreed-Upon Solution*

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- JTAG Switch Module (JSM)
  - Mounted on or near backplane as a plug-on module to backplane or as a specialized blade
  - Provides a JTAG Switch interface from each MCH and from an External Tester
  - Provides single TAP interface to each AMC
  - Provides single TAP interface from/to each MCH
  - Provides external TAP interface from External Tester
  - Allows for connection to each AMC individually
  - Provides “parking” of AMC in stable TAP states



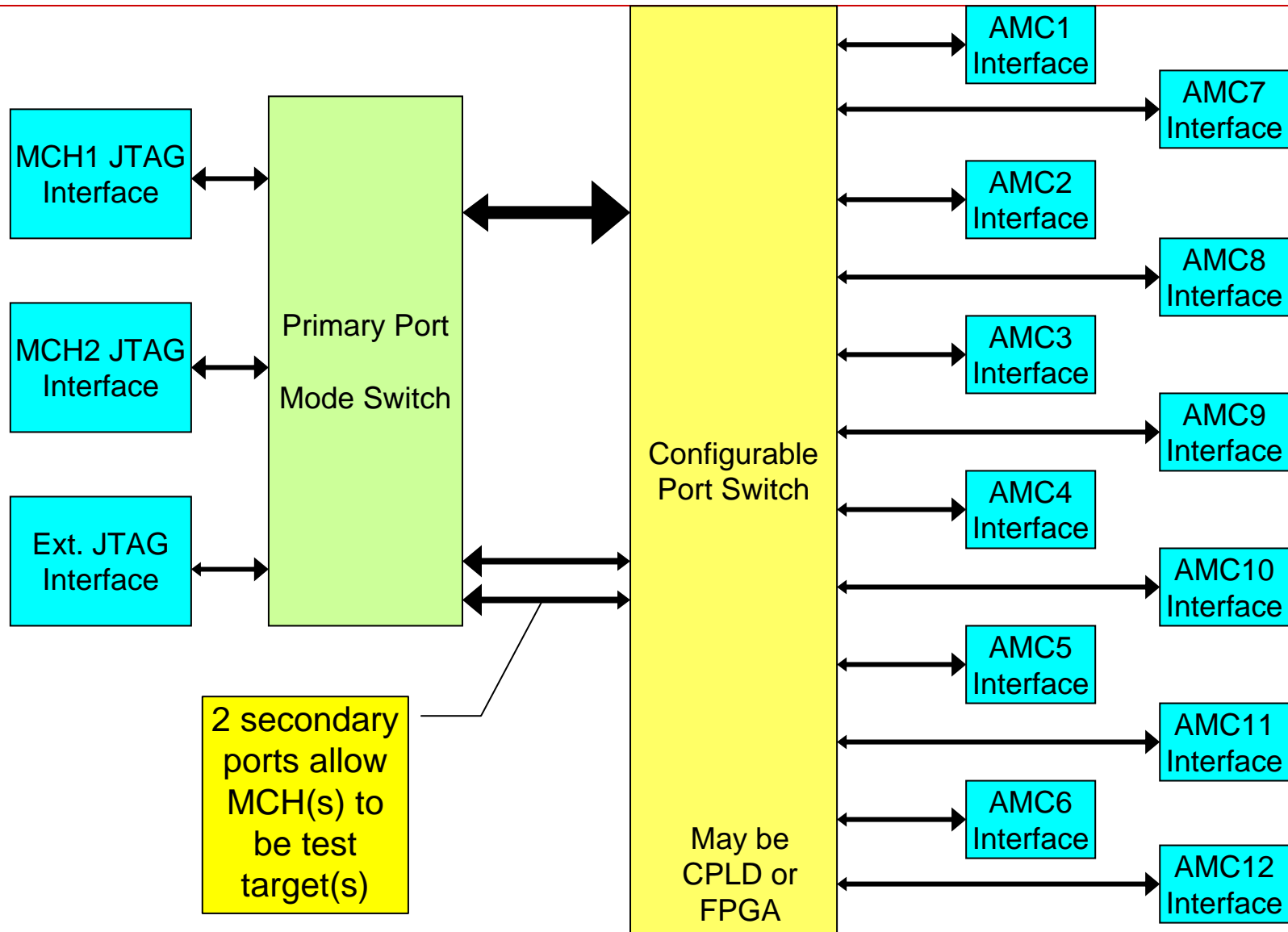
# Overview of the JTAG Switch Module

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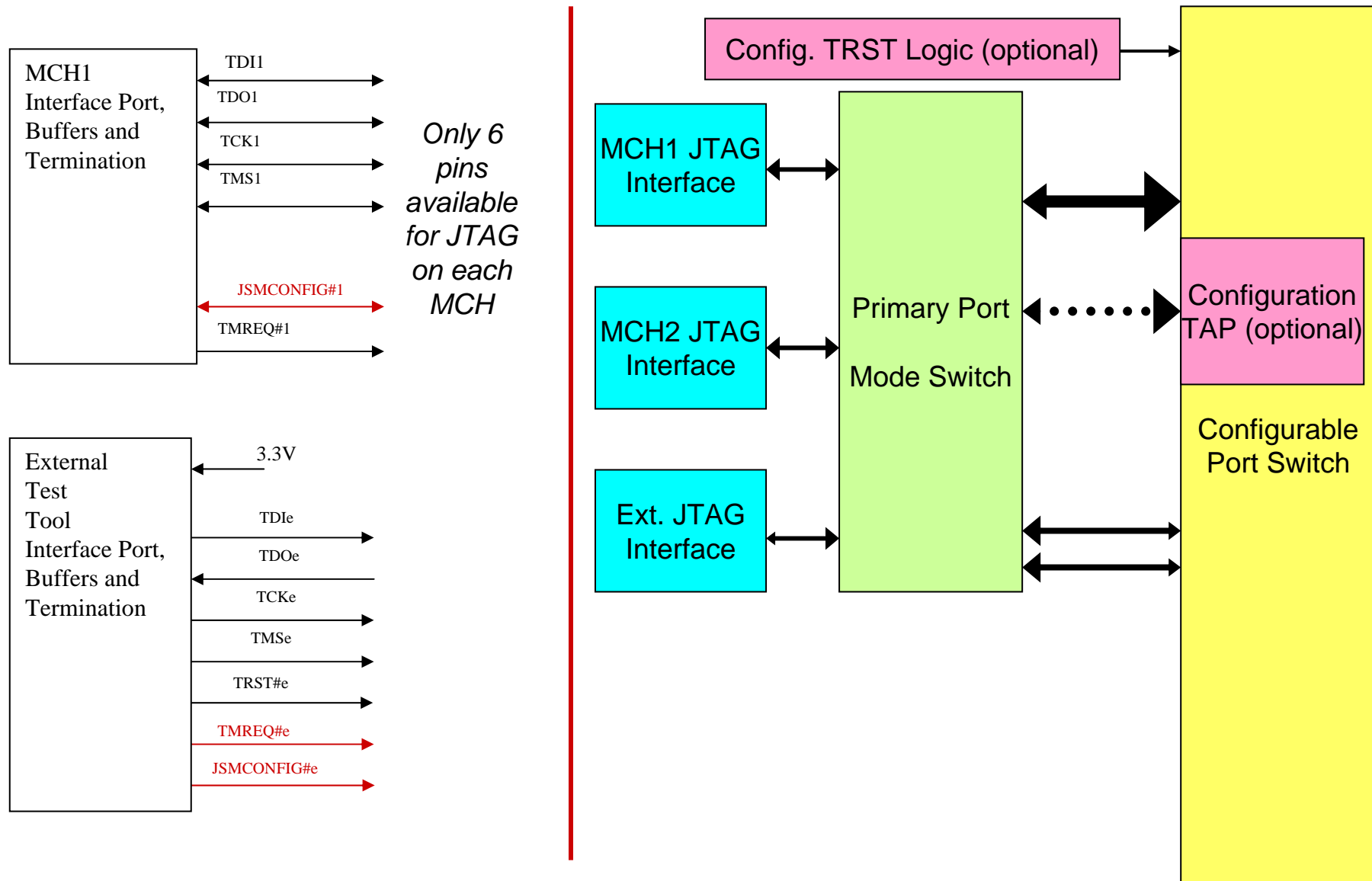
- Specification recommends a chain topography
- Specification does not mandate a specific design
- Specification does not mandate a specific control protocol
  - SPL, SCANBridge, ASP, other protocols could work
- Provides Configurable Star architecture on the back end
  - User programs a CPLD or FPGA for the Port Switch to implement the desired architecture for a given system configuration (e.g., Ring, Star, Hybrid)



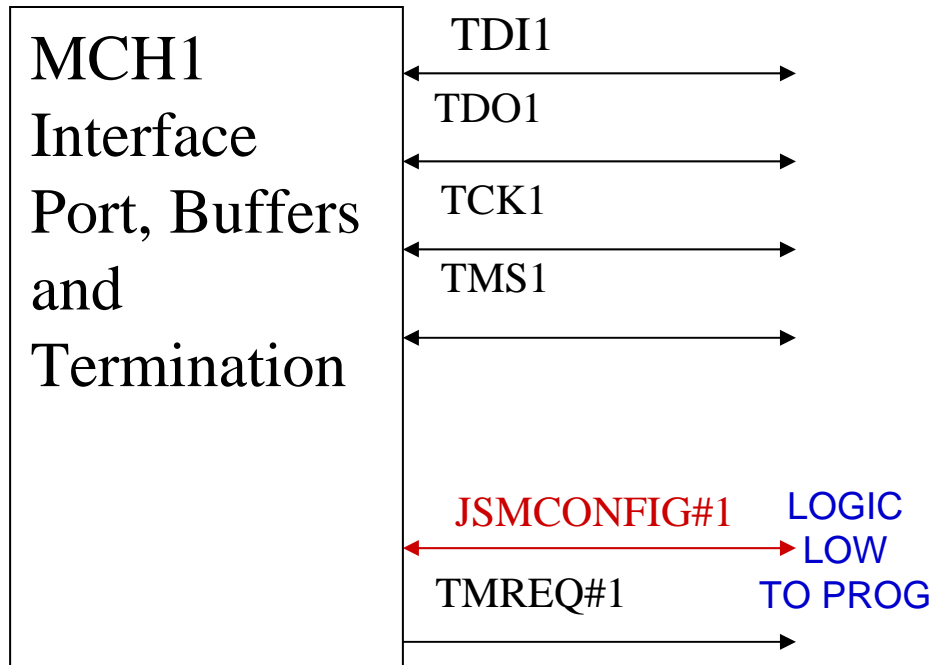
# Overview of the JTAG Switch Module



# Overview of the JTAG Switch Module



# Programming and Chain Selection Issues



## ■ Programming Issues

- MCH TAP is bi-directional
- Dual role for TRST# from MCH (Test Reset/ Programming of PS)
- Additional signal required from External Testers
- System-Test languages must support GPIO coordinated with scan operations (Test Reset/ Programming control)
- Programming not necessary if ASIC/ASSP design is used
- Secondary chains must be held in a default inactive state during programming of PS

# Programming and Chain Selection Issues

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## ■ Chain Selection Issues

- What selection protocol to use? TBD by the system builder
- ATPG tools must be able to support chosen protocol
- For slot independent architectures to support inter-slot testing, the Port Switch must be able to “park” a given slot in a stable TAP state on disconnection of the slot
- JSM must provide a way to perform global Test Reset
- JSM is not required to provide a broadcast state transition
  - MicroTCA architecture ensures that each blade can be brought up in an observe only mode – no conflicting signals
  - ATPG algorithms are constrained to drive from a single blade only

# Conclusions

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- Even with the **pin constraints** for MicroTCA, **System-Level JTAG is still possible**
- The JSM architecture provides the **same flexibility** that comes from a Multi-drop architecture to support **dynamic configuration** inherent to Hot Swap
- Since the **selection protocol is not governed** by PICMG there may be a **question of system compatibility** but, unlike the case with Multi-drop architectures, the MicroTCA-specified solution **ensures blade compatibility**
- The JTAG Switch Module is a Field Replaceable Module
- A **re-programmable Port Switch is not required** to support System-Level JTAG
- FPGA/CPLD vendors and ASSP vendors are beginning to design flavors of JSMs for use in MicroTCA