Design Patterns & Templates

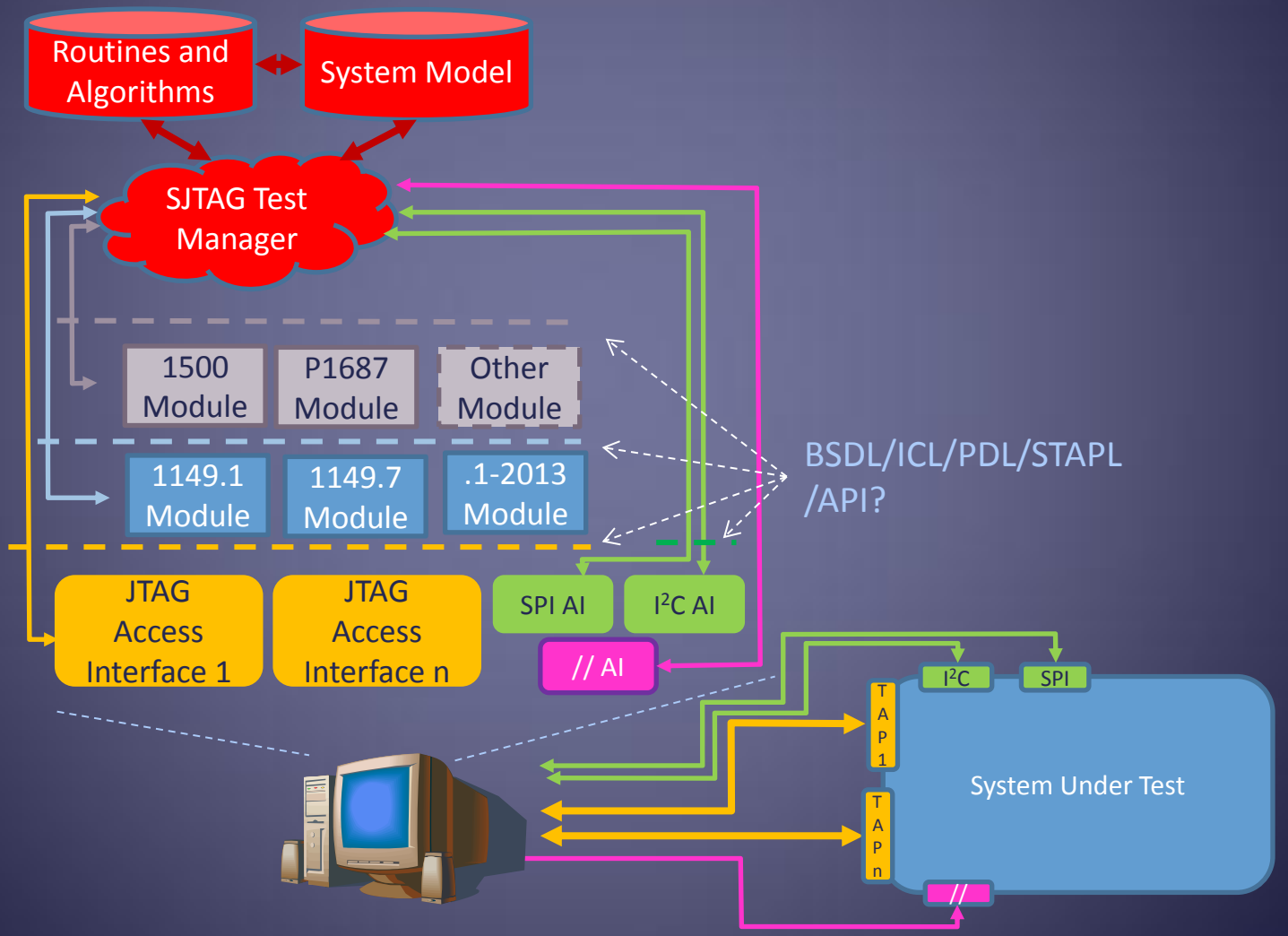
Defining SJTAG

- What makes something a “system”?
  - Multiple boards?
  - Functionality?
  - Design Hierarchy?
  - Where do SoCs fit in?
  - Need to manage resources (including chains)?

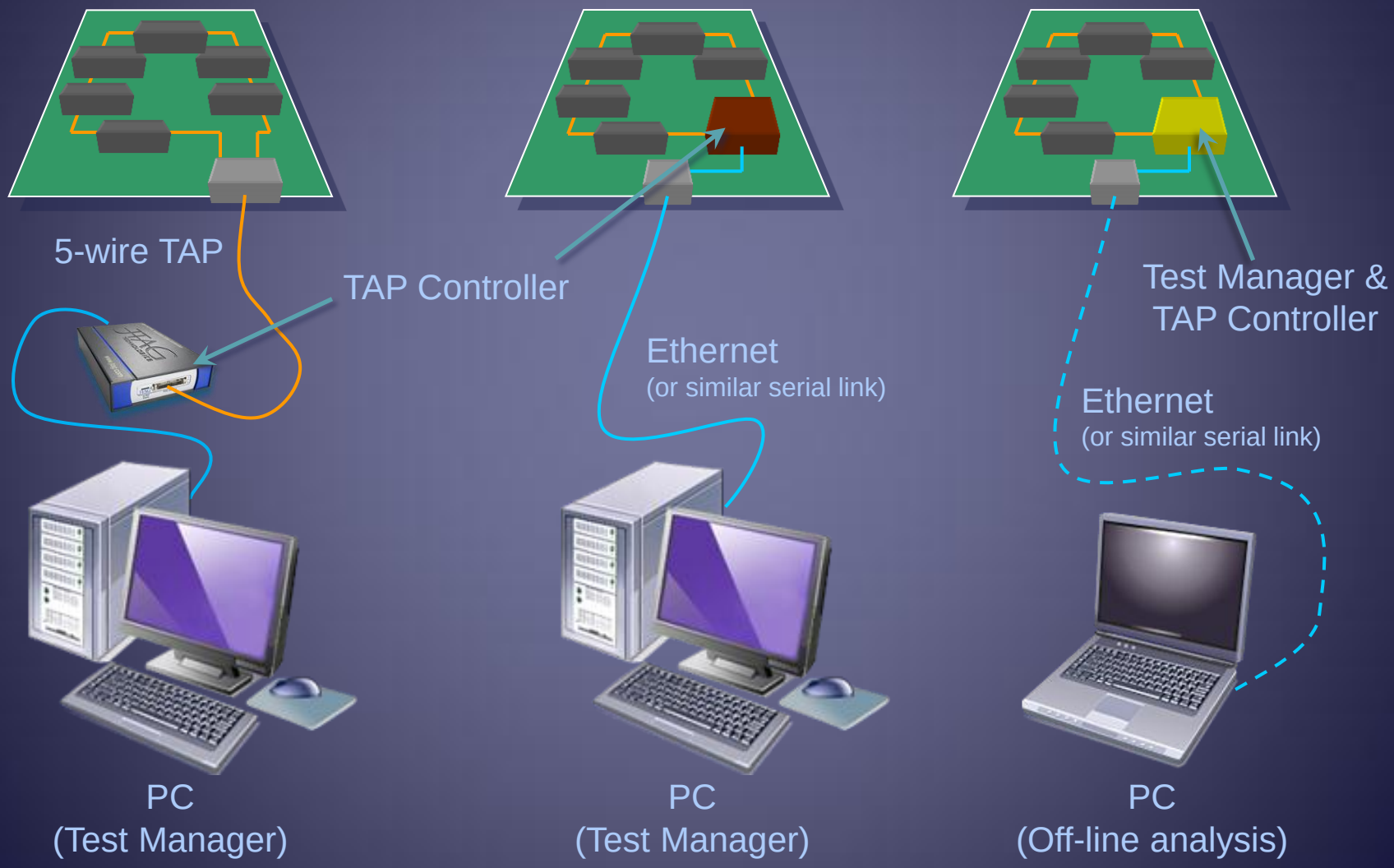
SJTAG vs JTAG

- Reuse of manufacturing tests:
  - Field service, hardware verification.
- Non-traditional applications:
  - Fault injection, software debug.
- Standardize the minimum set of information needed to run a test:
  - Allow a COTS board to be tested within a system.
- Instrument coordination across devices:
  - Not really addressed by P1687 or 1149.1-2013.

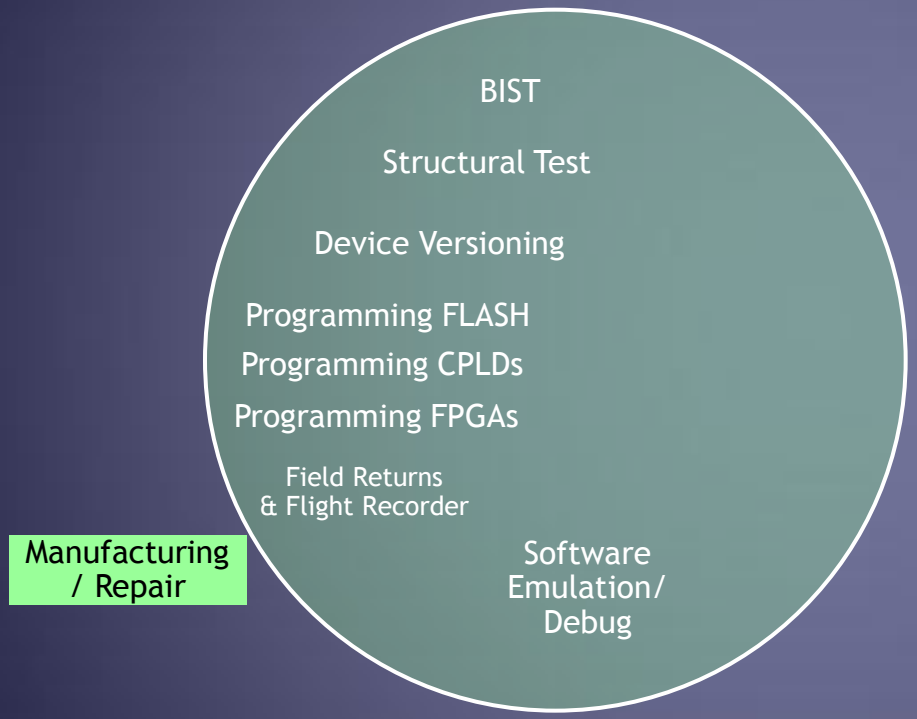
SJTAG Visualization



External to Embedded

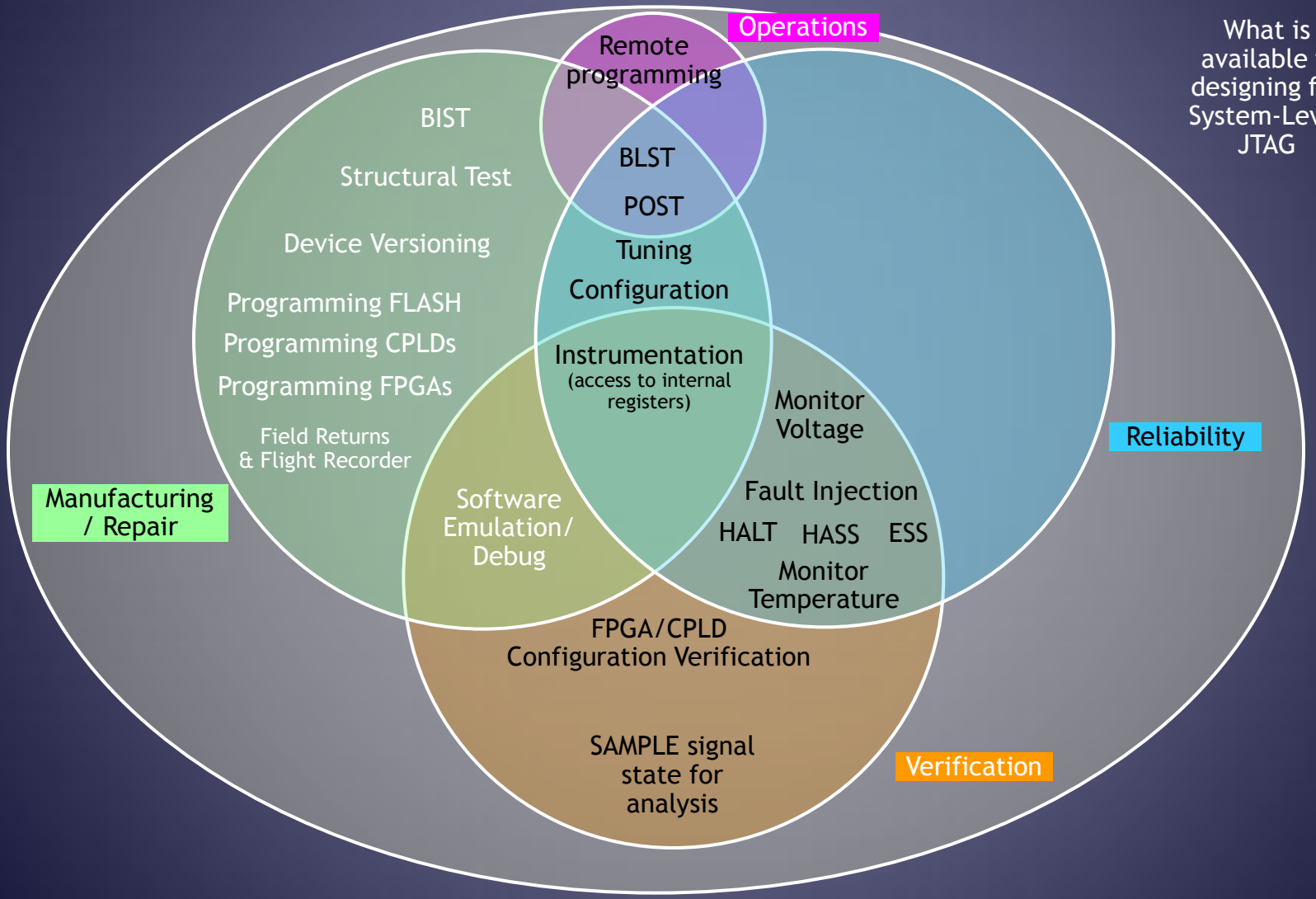


Traditional Boundary-Scan Universe



- Scoped to board level testing
- Evolved to be used for more than just structural test
- External access to boards from PCs and bed of nails testers
- Driven by manufacturing needs

SJTAG Universe

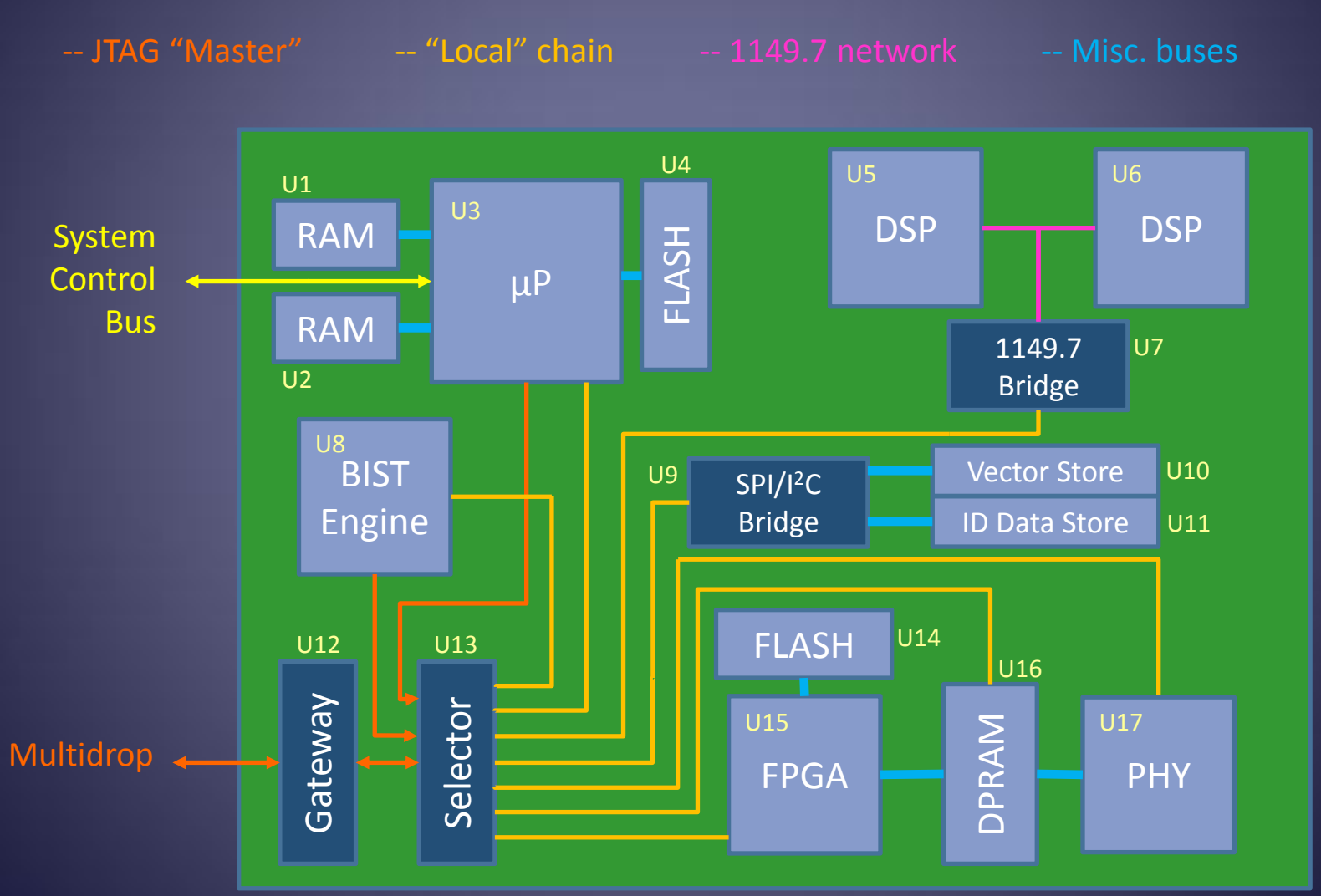


What is available if designing for System-Level JTAG

Design Patterns

- Taken from the field of architecture.
- Classifies a problem space by recording a set of key characteristics that define it.
- Problems that share the same set of characteristics will also share the same solution *method.*
- Description of each problem and its characteristics are stored as “Templates”.

Illustrative System



SJTAG Templates

- Go/NoGo Memory Structural Test based on boundary-scan access from Host
- Go/NoGo Structural Test of AC Coupled Links
- Go/NoGo Instrumented Test of AC Coupled Links with a Single Loopback at One End
- Go/NoGo Instrumented Test of AC Coupled Links with Multiple Loopbacks at One End
- Go/NoGo Instrumented Test of AC Coupled Links with One Device Tx and One Device Rx

Template Example

- **Go/NoGo Instrumented Test of AC Coupled Links with Multiple Loopbacks at One End**
- **ANALYSIS DESCRIPTION NAME**
  - Go/NoGo Instrumented Test of AC Coupled Links with Multiple Loopbacks at One End
- **ANALYSIS DESCRIPTION IDENTIFIER**
  - TBD
- **OPERATION OVERVIEW BEING ANALYZED**
  - testing assembly connectivity for correctness, including placement, orientation, correct device, basic "aliveness", shorts and opens.
  - a table for the PCOLA/SOQ would be useful at this point, and should be part of the template.
  - focus is on detection of a failure, not diagnosis for the defect.
  - test based on predetermined AC pattern from U5 or U6 and reflected back from the other device.
  - reflected data may be returned on one or more lanes to aid diagnostics:
    - One transmit lane paired to one receive lane, where either the transmit or receive lane in use can be varied (point-to-multipoint and multipoint-to-point)
    - One transmit lane to multiple receive lanes simultaneously (broadcast)
    - Multiple configurations may be used within a test to enhance diagnostics and isolation in the presence of single faults
  - intent is to confirm that a data eye can be established.

Template Example (2)

- **DESIGN TARGETED**
  - U5/U6 circuit block.
- **USE CASE TARGETED**
  - Structural Test (ST)
  - ~~Configuration / Tuning / Instrumentation (CTI)~~
  - ~~Software Debug (SD)~~
  - ~~Built-In Self Test (BIST)~~
  - ~~Fault Injection (FI)~~
  - ~~Programming / Updates (PU)~~
  - ~~Root Cause Analysis / Failure Mode Analysis (RCA/FMA)~~
  - ~~Power-on Self Test (POST)~~
  - ~~Environmental Stress Test (EST)~~
  - ~~Device Versioning (DV)~~
- **PRODUCT LIFE CYCLE STAGE ADDRESSED**
  - Post-assembly Manufacturing Test
  - **Harrison's note:** Important aspect is that this is a case of reuse of something developed for NPI.

Template Example (3)

- **INHERITANCE**
  - None yet.
- **ASSUMPTIONS**
  - U7 addressing is properly configured to access U5 and U6.
  - Any compliance enable condition can be set from some boundary scan controlled IO port, e.g on U15 or U7.
  - power is supplied to the DSPs(U5, U6) and Bridge (U7), the Gateway (U12), and the Selector (U13); (could go under DEPENDENCIES)
  - Any ICE/debug port is not conflicting with boundary scan access.
  - Necessary instrumentation is provided either as soft core or hard core within the DSPs.
  - Instruments are controllable through the 1149.7 port on each DSP.
  - Remote device provides a means to loopback a pair of lanes to the source device for testing,
  - Receive and transmit instruments reside within a single device.
  - The state of the transmit, receive and loopback instruments, including the lanes to be used, is known to and controlled by the Test Manager.
    - The state may be set through JTAG or some other interface (e.g. I^2C, SPI, etc.) that is under the control of the Test Manager.

Template Example (4)

- **DEPENDENCIES**
  - power pins have been tested for shorts prior to this test;
  - any 1149.1 compliance enable pins for U5 and U6 are controllable by the host tester (DFT requirement);
  - Scan chain is designed so that the selector has access to U7(DFT requirement);
  - Scan chain connectivity to U5, U6 and U7 has been verified prior to this test;
- **OPERATIONAL LEVEL REQUIRED**
  - Out of Service
- **JTAG TECHNIQUES USED**
  - IEEE 1149.6 interconnect testing (U5 and U6)
  - IEEE 1149.1-2013 (example C.5) interconnect testing using instrumentation IP (U5 and U6)
- **TEST ACCESS POINT**
  - Gateway (U12), accessing U5 and U6 through the Selector (U13) and Bridge (U7).
- **TEST CONFIGURATION REQUIRED**
  - Only needed scan chain for this particular test would be the one from the Selector to U7 (translating to U5 and U6), unless compliance enable or other constraints are controlled by boundary-scan devices in other chains

Template Example (5)

- **CONSEQUENCES**
  - Can be used for AC coupled nets.
  - Supports testing of links at the board edge.
  - Requires a means of coordination between Rx and Tx instruments.
  - Diagnostics can be provided down to a single lane:
    - Multiple transmitters permit isolation to a TX lane provided that the common Rx lane is functional.
    - Multiple receivers permit isolation to a RX lane provided that the common Tx lane is functional.
- **SIMILAR DESCRIPTIONS**
  - Go/NoGo Instrumented Test of AC Coupled Links with a Single Loopback at One End
- **SIBLING DESCRIPTIONS**
  - Go/NoGo Instrumented Test of AC Coupled Links with One Device Tx and One Device Rx

Discoveries

- Insights:
  - Need to take care to avoid “template explosion”
    - Do you need a new template or just a note of things that need to be considered?
  - May need to manage more than TAP interfaces.
  - Tests may not be Go/NoGo
    - Depends on how you treat the results.
- Questions:
  - How do we express software tooling requirements?
  - How do we make diagnostics portable?