Test Managers and Controllers in the SJTAG Domain

Discussion

Insights of Modularity

- "An implementation of an SJTAG architecture in a system allows Test Programs, running on Test Controller(s), to operate on Bscan controlled Functions in Bscan enabled components."
 - Gunnar Carlsson, Ericsson, former SJTAG Vice-chairman

Layers of Software

Test Manager



Test Controller

Application

Test Package and Test
Program Flow Control (Ordered
collection of Test Programs)

Test Programs and Test Step Flow Control (Ordered collection Of Test Steps)

Test Steps (Ordered collection of Scan and PIO Operations)

1149.1 Scan Operations (Represents Leaf Functions as Vector Patterns)

Test Access Port Controller Operations

- Avoid thinking in terms of "hardware":
 - Capabilities may co-reside within the same hardware or may not but will retain their own distinct "role" in either case.
- There are defined interface boundaries between each layer.

Green lines show interface boundaries.

Definitions

- SJTAG Manager: A term used to describe any combined hardware/software SJTAG Control System that is used as a freestanding or integral on-line runtime controller providing top-level management of UUT test or configuration operations.
- Control System: A term used to describe any combined hardware/software entity that provides control of the execution of some part of the application. Multiple Control Systems may exist and responsibility may be delegated from one to another in a hierarchical manner.
- Test Step: A singular operation for which the next highest level in the control hierarchy is able to resolve control.

An Example – EST Case

External Controller

Test Manager

SJTAG Manager

Test Step Controller

JTAG Control System I²C Control System

SPI Control
System

Chamber Manager

JTAG Chains

I²C Access Links SPI Access Links

UUT

EST Chamber

Thermal Controller

Fans Heater

Chiller

Temp. Sensor

JTAG Control System

JTAG Control System

Test Step Interface

Test Controller

Vector Sequencer

JTAG Test Controller Interface

TAP Master Hardware

 JTAG Control System shown as example

 Similar model applies to all other "Control Systems"

The Test Manager Problem

Test Manager



Test Controller

- Since the transition from Test Manager to Test Controller is determined by architecture, how do we know the capability of each?
 - Can we break this down into more deterministic parts?
 - Does the Test Manager subsume some of the lower level entities or interface to them?
- If we say the SJTAG Manager is responsible for all operations within the SJTAG domain, how do we interface to other domains?
 - Can, or should, the SJTAG Manager take the "overseer" role?
 - Is there always an "overseer"?