



**Minutes of the
SJTAG Fringe Meeting at EBTW'06
Wednesday 24 May, 2005
Chilworth Manor, Southampton, UK**

Attendees

Jukka Antila, Nokia Networks, FI
 Patrick Au, IBM, UK
 Mick Austin, JTAG Technologies, FI
 Maria Back, ASSET InterTech, UK
 Ben Bennetts, Bennetts Associates
 (SJTAG Chairman), UK
 Gunnar Carlsson, Ericsson, Sweden
 Pete Collins, ASTER Ingenerie, FR
 Bill Eklow, Cisco Systems, USA
 Billy Fenton, International Test
 Technologies, IR
 Kevin Fotheringham, ASSET InterTech,
 UK
 Steve Harrison, Motorola Networks, UK
 Ville Hassinen, Ericsson, Sweden
 Jan Heiber, Goepel, DE
 Peter Horwood, Firecron, UK
 Frans de Jong, Philips, NL
 Artur Jutman, Technical University Tallinn,
 Estonia

Thomas Kronqvist, Saab Test Systems,
 SW
 Erik Larsson, Linköpings Universitet,
 Sweden
 Adam Ley, ASSET InterTech, USA
 Christophe Lotz, ASTER Ingenerie, FR
 Markku Moilanen, Oulu University, FI
 Eugene Mullen, Firecron, UK
 Franc Novak, Josef Stefan inst., Slovenia
 Larry Osborn, ASSET InterTech
 Anthony Sparks, JTAG Technologies,
 USA
 James Stanbridge, JTAG Technologies,
 UK
 Bernard Sutton, Robot, UK
 Reg Waller, ASSET InterTech, UK
 Jim Webster, Consultant (ex-BAE
 Systems), UK
 Thomas Wenzel, Goepel Electronic, DE

Agenda

Agenda for the SJTAG meeting at EBTW'06.

1. Ben Bennetts, SJTAG Chairman: Introduction and status of SJTAG.
2. Views from the industry
 - 2.1 Test manager vendors. Adam Ley, ASSET InterTech, USA
 - 2.2 Systems industry. Steve Harrison, Motorola, UK
 - 2.3 Scan support device vendors. Peter Horwood, Firecron, UK

3. Summary and wrap-up. Ben

Firecron will be demonstrating and initial proof-of-concept of SJTAG's ideas

This live demo will show ASSET's ScanWorks product controlling the application of a variety of STAPL actions on a Firecron FSC1000 demo board. The board will allow remote test execution & diagnostics via a LAN or WAN interface. The demonstration will show delivery of the STAPL commands onto a local Firecron Digital I/O card (one that is next to the ScanWorks station) and onto a similar board that is remote (based on a link set up over the Internet).

Presentations

Test manager vendors. [Adam Ley](#), ASSET InterTech

Systems industry. [Steve Harrison](#), Motorola

Scan support device vendors. [Peter Horwood](#), Firecron.

Discussion

The demonstration provoked much discussion, as it was designed to do – what am I really looking at?, how does this portray the concepts of System JTAG?, etc. Basically, what it showed was delivery and return of test vectors via an Ethernet connection. Original delivery format was SVF. Return format was in a Firecron binary format called BVR. The pattern generator was ASSET's ScanWorks, but could be any generator that produces vectors in SVF format. The receiving test manager was also ASSET's ScanWorks but could be any station that understands BVR. The board-under-test was a combination of Firecron's FSC-1000 controller connected to ASSET's ScanLite demonstration board.

We discussed how to proceed, based on the proposed [action list](#) from Steve Harrison's presentation. This list is shown below, along with the names of the people who agreed to pick up the action. Not every action has a name yet. Feel free to volunteer.

Actions

| Action Item | Name | Deliverable | Date |
|-----------------------------------|-----------------|-----------------------------|------|
| SJTAG Project Manager | Jim Webster | SJTAG Project Specification | ASAP |
| Vector/Sequence definition | Anthony Sparks | | |
| Scan Chain definition | Steve Harrison | | |
| Vector return definition | Adam Ley | | |
| Net and component list definition | Jim Webster | | |
| Physical Layer | | | |
| System configuration files | | | |
| System security | | | |
| SJTAG manager requirements | | | |
| Use scenarios | Gunnar Carlsson | | |
| Diagnosis | Christophe Lotz | | |
| Future demos | Ben Bennetts | | |

I have had a go at defining the things we need to think about as we [build the demonstrations](#). The ideas follow. Feel free to comment.

In the meantime, I will work with Jim Webster to get the SJTAG project specification in place, calling on those who have volunteered to pick up some of the actions above.

Any questions, or comments, e-mail me at ben@dft.co.uk

Ben Bennetts
SJTAG Chairman

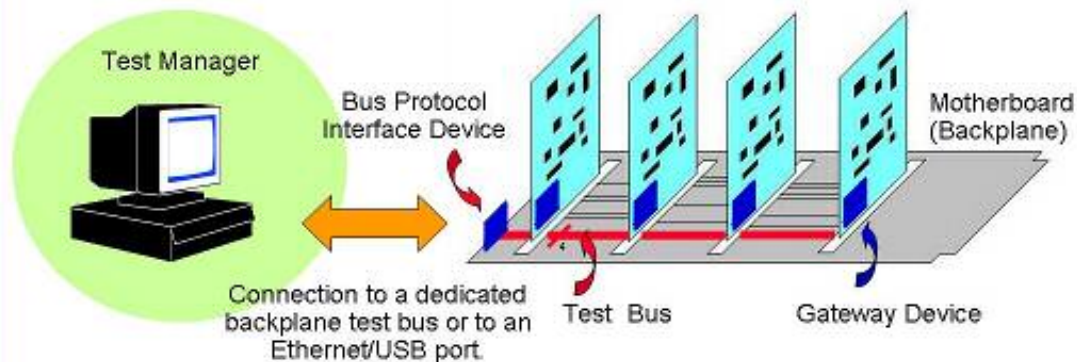
SJTAG Demonstrations



Possible Demonstration Scenarios Version 1 27 May 2006

Ben Bennetts (SJTAG Chair)

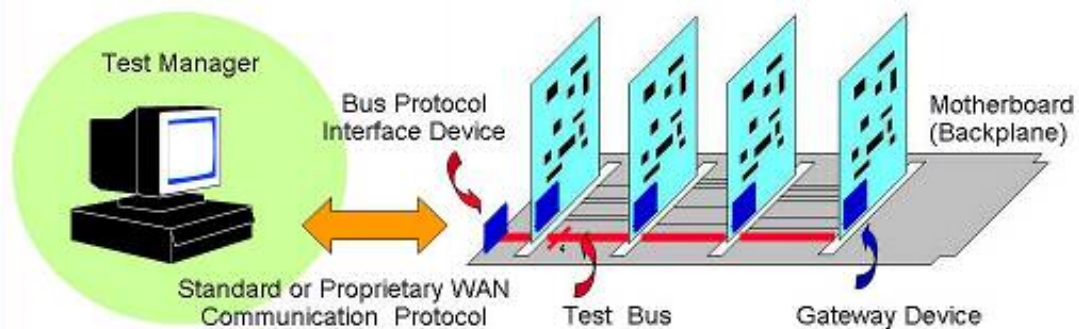
Reminder: System Test Use Scenarios



- Prototype system debug prior to volume manufacturing of the system.
- Manufacturing test, prior to customer shipment, especially in an Electronic Manufacturing Services/Contract Manufacturing environment where testing may be carried out by lower-skilled technicians or ATE operators.
- On-site customer installation and commissioning + in-service field-service calls.
- Repair depots.



Reminder: eXternal Boundary Scan Test (XBST)



Test Manager provides:

- Learning the configuration of the system: what UUTs are present, in what slots, etc
- Creating (off-line) and applying (on-line) an overall UUT and system test plan
- Response capture and analysis
- Overall control of all test and config operations

"Bare bones" implementation

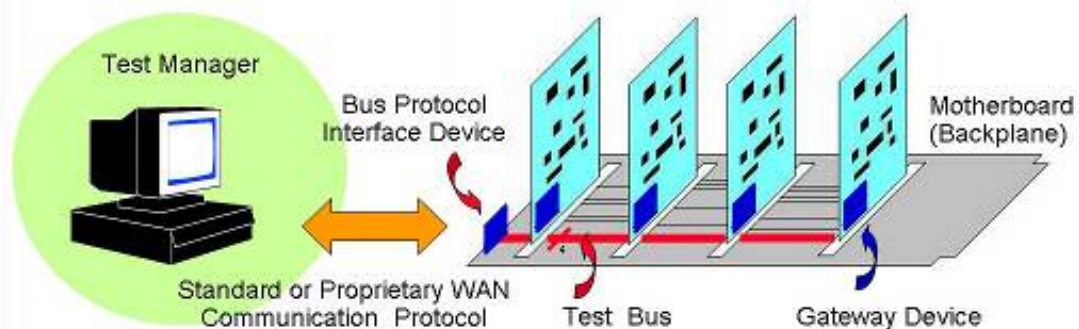
- Backplane access (Ethernet, USB, etc)
- UUT addressing scheme e.g. a gateway device.

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SJTAG-Demos ppt, V1

Side 3



Reminder: Embedded Boundary Scan Test (EBST)



Test Manager provides:

- Overall control of embedded test and configuration sequences: data load, start, results capture, logging, analysis and display

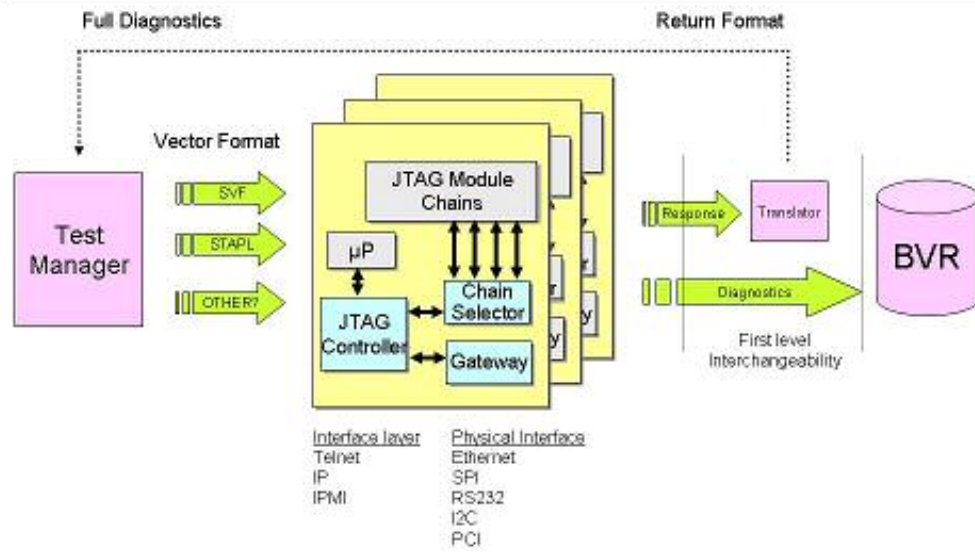
"Fully-loaded" implementation

- Backplane access (Ethernet, USB, etc)
- UUT addressing scheme e.g. a gateway device
- Embedded Test Controller with or without a separate JTAG Protocol Manager
- On-board path selection, if required.

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SJTAG-Demos ppt, V1

Side 4

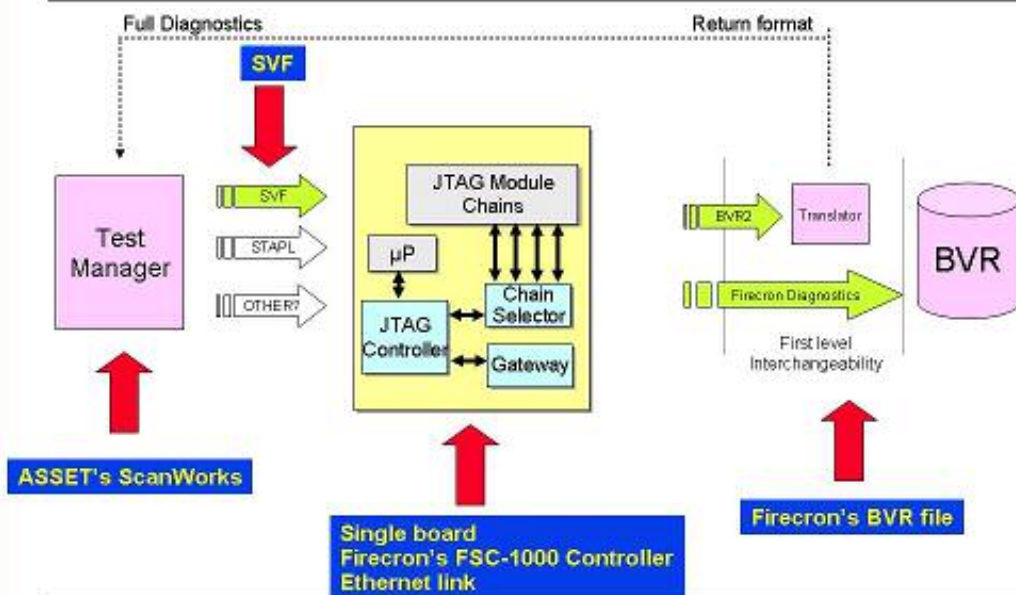
SJTAG The General Demonstration Scenario



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Slide 5

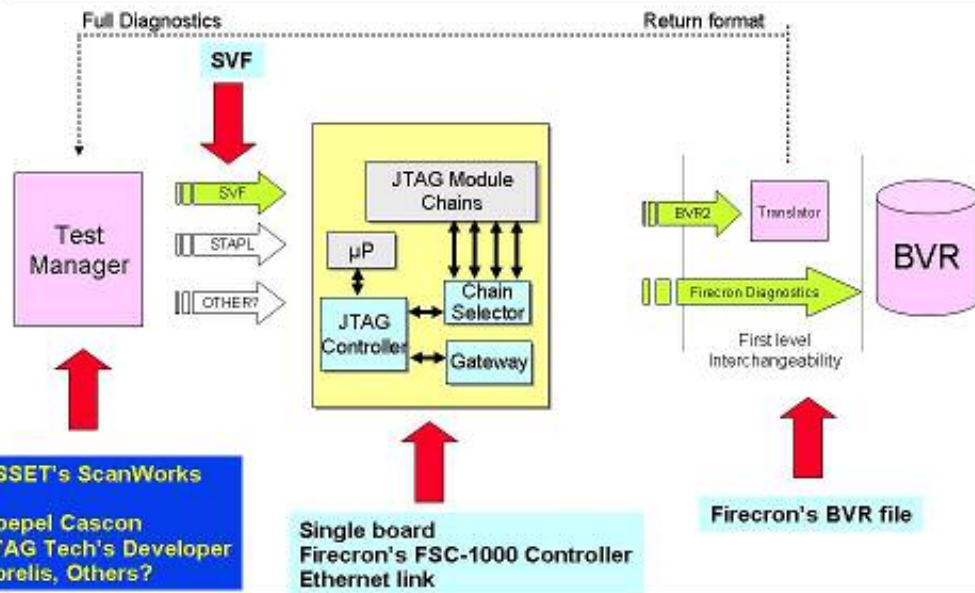
SJTAG Demo 1: Shown at EBTW May 2006



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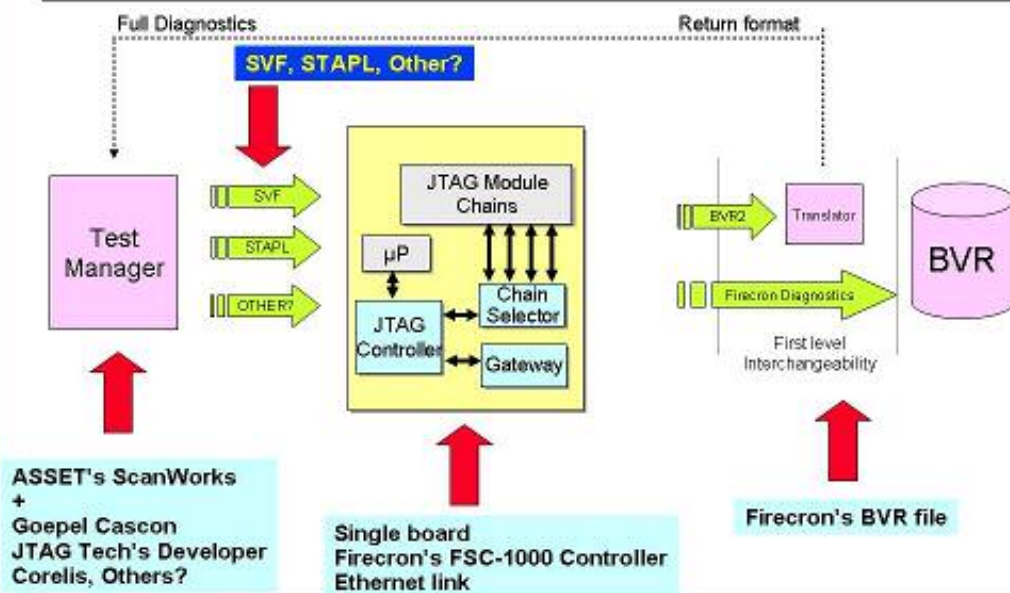
Building the Demos: Test Manager



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Slide 7

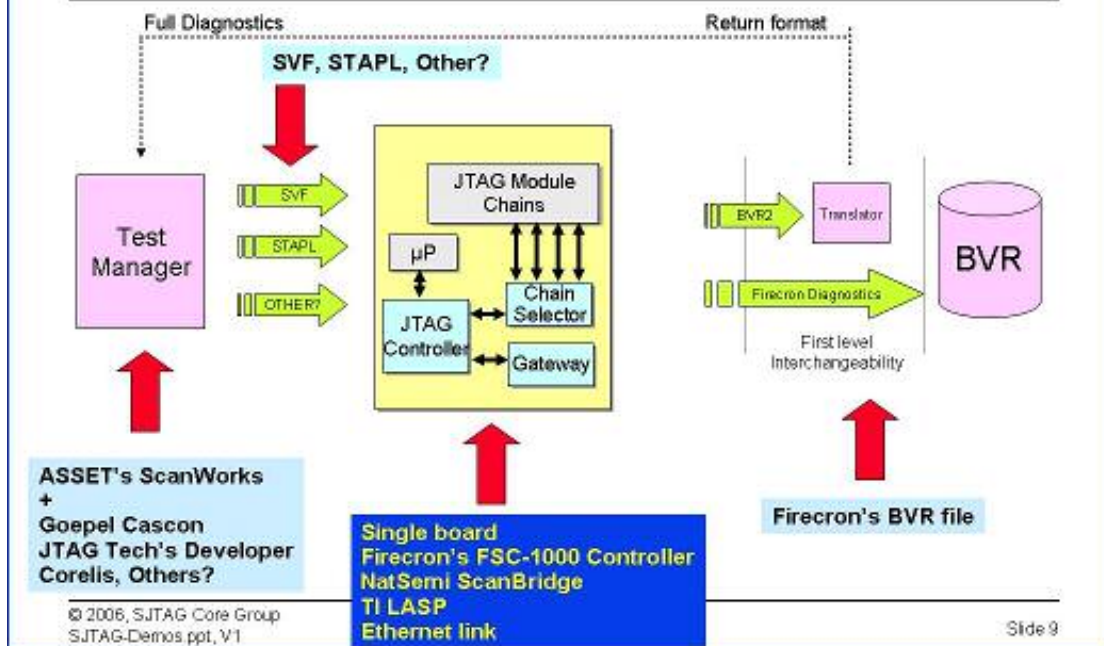
Building the Demos: Input Language



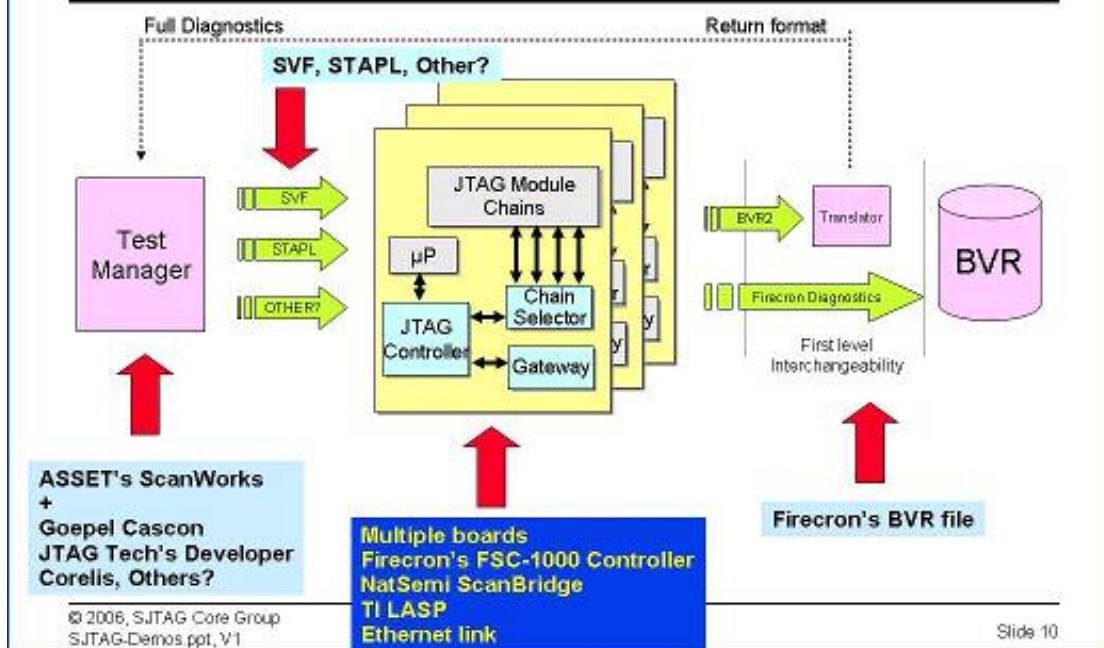
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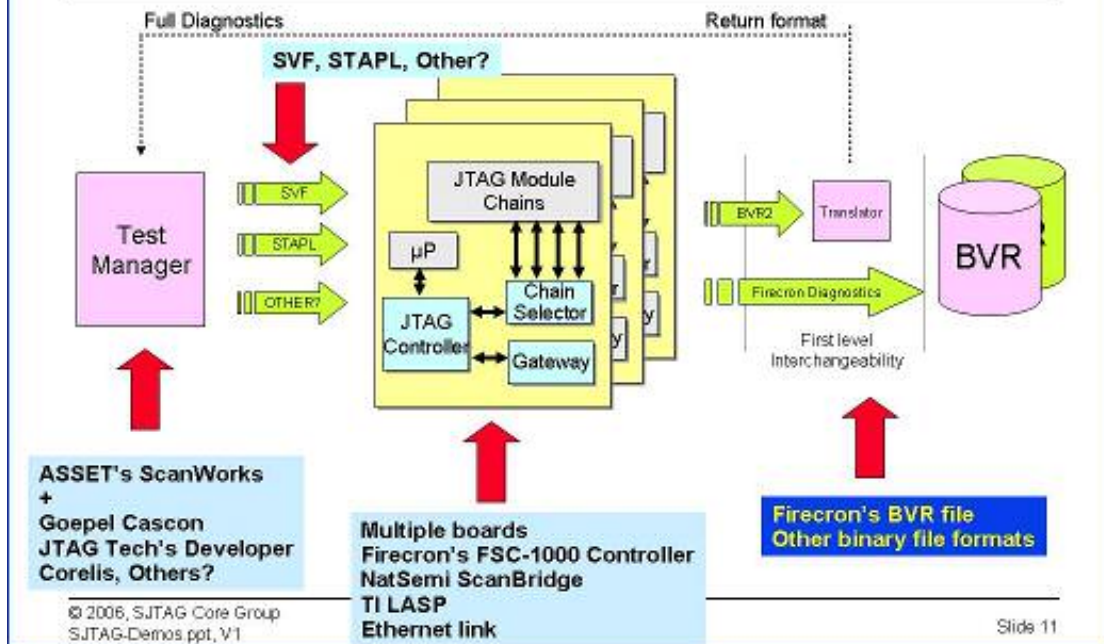
Building the Demos: JTAG Controller



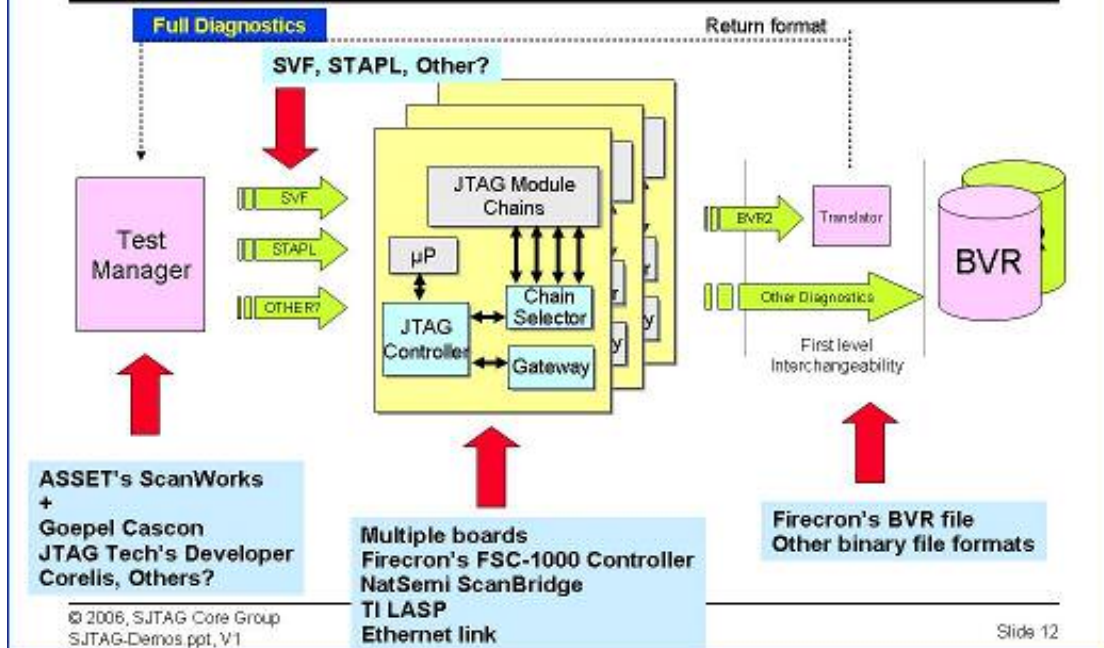
Building the Demos: Multiple Boards



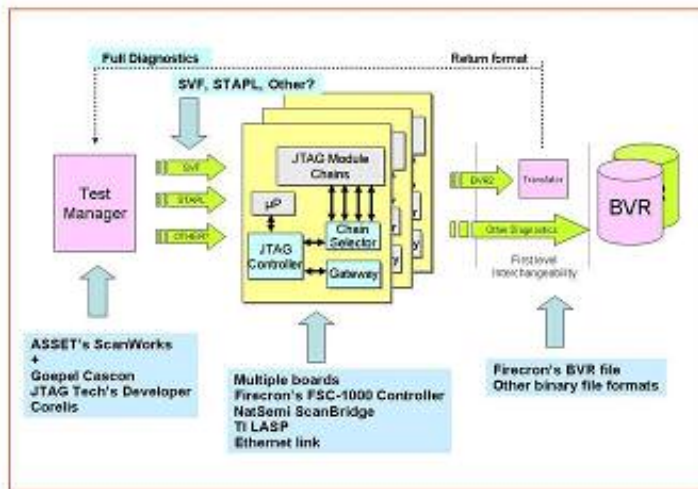
SJTAG Building the Demos: Return Format



SJTAG Building the Demos: Diagnostics



Adding Use Scenario Considerations



- Prototype system debug.
- Manufacturing test,
- On-site customer installation.
- In-service field-service calls.
- Repair depots

What Next?

- Define as a Demo Build project to include a sequence of staged demonstrations, with timelines and committed help.
- Include lower-level detail as per 24 May 2006 minutes
- Target show opportunities in 2006:
 - Board Test Workshop, September 14 – 15, Fort Collins, CO
 - ITC, Oct 30 – Nov 3, Santa Clara, CA

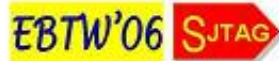


EBTW'06 Presentation
Adam Ley, ASSET InterTech



A perspective on SJTAG
from a "test manager" (tools) vendor

Adam W Ley
ASSET InterTech, Inc.



"There are 10 kinds of people ..."

"There are 10 kinds of people in the world. People who understand binary numbers, and those who don't."

- unknown

(with acknowledgement to Ken Parker,
whose email signature first brought it to my attention)

“The secret is to ask the right question. Then the answer takes care of itself.”

- unknown

(with acknowledgement to Carl Barnhart,
whose email signature first brought it to my attention)

- What is SJTAG?
- Or, What does SJTAG want to be when it grows up?
- And, just as important (perhaps more), What is SJTAG *not*?

- One (baby) step at a time ...
- ... crawl before walk ...
- ... walk before run ...

- Consortium?
 - Corporate buy-in?
 - "Just" a group of individuals (no offense intended)?

□ White paper?

- Clearly
(see www.dft.co.uk/SJTAG/SJTAG_white_paper_0.4.pdf)
- Defining terms, etc.

□ Standard(s)?

- Presumably, at some point ...
- But what (first)
- And for whom

Architecture?

- "Backplane" test bus
- "JTAG" or *not*
- Multidrop
- Full star
- Hybrid

Silicon support devices?

- Gateways
- Linkers
- Etc.

Test manager tools?

- Generation
- Application
- Diagnostic

 Description/ Data Format(s)?

- Existing
- Existing with Modification
- Purpose-built

Transport?

- Application layer

...

- Higher layer

 Design? Manufacture? Field Service? Repair?

Local?

Remote?

eXternal?

Embedded?

All of the above???

- YES??
- But, remember the caution ...

 Issues/ Concerns

- Security?
- Others?

- Generation?
- Application?
- Diagnostic?
- Other?

- Hopefully just the beginning of a beautiful relationship ...

EBTW'06 Presentation
Steve Harrison, Motorola



MOTOROLA NETWORKS

System JTAG
 24th May 06 Southampton

Presented By
Stephen Harrison
 steve.harrison@motorola.com

System JTAG a Motorola Perspective

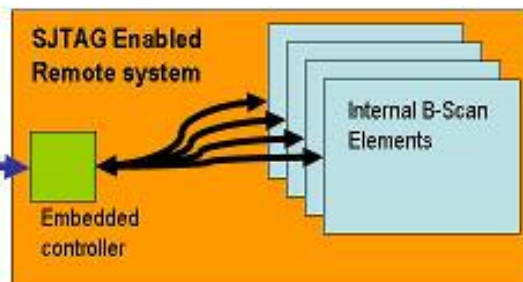


"System JTAG"

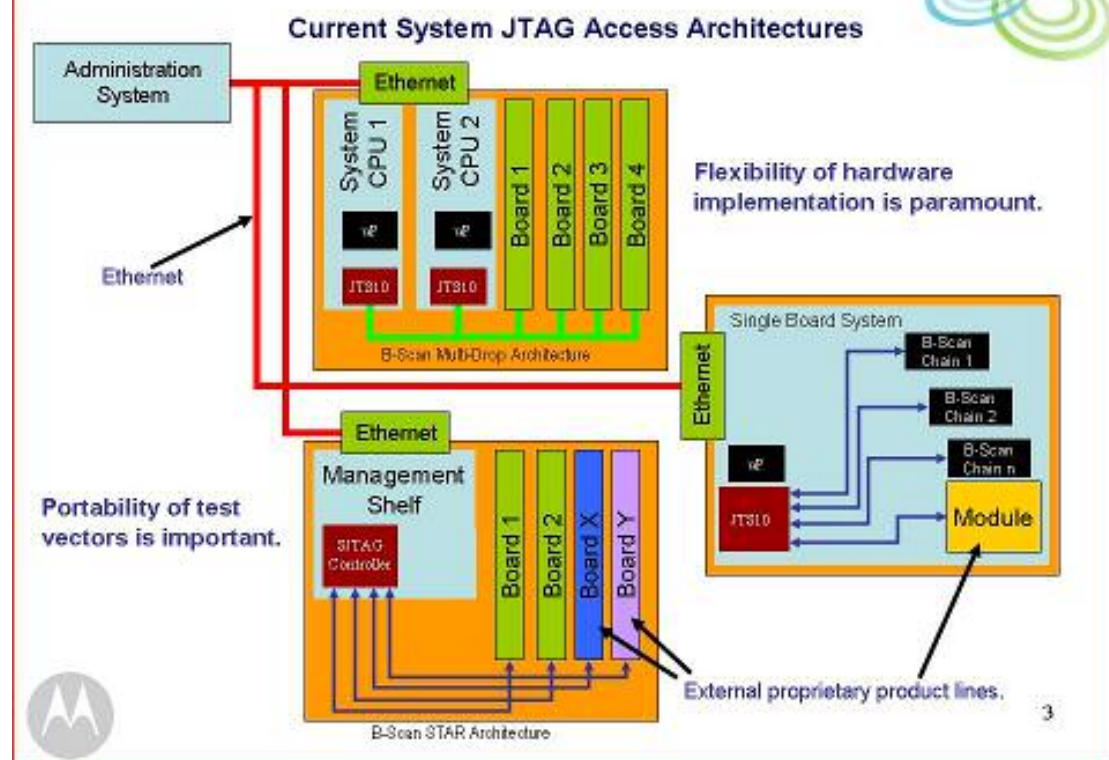
Motorola's perspective on SJTAG can be summed up as :

The ability to describe, execute and diagnose any Boundary-Scan test or programming action in an agreed industry standard format on a SJTAG enabled system.

SJTAG Manager
 Diagnostic and Repair centre



System JTAG a Motorola Perspective



SJTAG a Motorola Perspective

**Motorola uses a proprietary SJTAG solutions now.
So why do we want a standard?**

For the following reasons:

- Aids adoption and growth of SJTAG design features
- Growth in multi vendor card solutions within a single cage requires a unified test model
- Improved flexibility, mobility and reuse of test solutions
- An enabler to future B-Scan use other than just test
- Improved third party support and tools
- Reduces in-house development and support costs
- Enables B-Scan market growth into new areas
- Provides a framework for products and designs to adopt

In essence a standard will reduce the overall cost of implementation through the use of off the shelf tools and practices.

SJTAG a Motorola Perspective



What is the key element of SJTAG?

There are many views to this question depending on who you ask.

However we feel that SJTAG is predominantly a "Software" issue and is NOT a Hardware and Architectural one.

- The vector transport system is immaterial between the SJTAG manager software and the embedded SJTAG controller , it could be I²C, SPI, Ethernet, USB or TTY.
- The target system B-Scan architecture is inconsequential, be it Multi-Drop, Star, etc.
- The target board may or may not have B-Scan chain control devices on.

Our major concern is that the embedded SJTAG controller solution can execute and return test vectors in a standard format for external SJTAG manager tool to interpret.



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SJTAG a Motorola Perspective



What is an embedded SJTAG Controller?

An embedded SJTAG controller can be

- A dedicated SJTAG controller device.
- A microprocessor attached to a B-Scan controller device e.g. JTS10
- A microprocessor that drives an IO port
- A custom FPGA/cPLD design
- Or a combination of any of the above

The SJTAG definition should not tie down or restrict the hardware implementation as this directly affects cost which in turn is a key barrier to SJTAG adoption.

Some SJTAG controller implementations may be fully featured, performing on board interpretations of SJTAG formats, while others run and return a native controller format to software modules on the remote SJTAG Manager to convert to the SJTAG format.



Flexibility is the key to hardware implementation

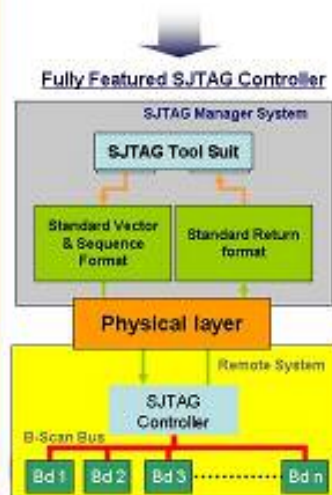
6

System JTAG a Motorola Perspective

Software Access Models

Fully Featured SJTAG Controller Model

This model assumes that the embedded SJTAG controller has sufficient resources to interpret, run and report test data back to the SJTAG manager directly in SJTAG format.

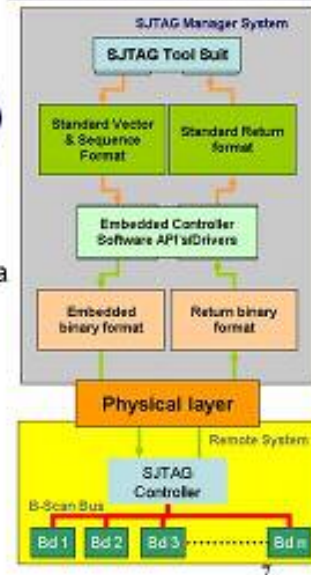


Reduced Featured SJTAG Controller Model

This model assumes that the embedded SJTAG controller doesn't have resources to interpret, run and report test data back to the control system directly in SJTAG format and relies on software drivers to convert the controllers native format to SJTAG format.

This model allows existing system B-Scan controller devices to support the SJTAG standard.

Reduced Featured SJTAG Controller



System JTAG a Motorola Perspective

SJTAG Diagnostic Requirements

The aim of SJTAG is to provide a portable set of test/programming actions that can be applied to remote units. This will become increasingly important with multi-vendor cards within a single unit with test generated from different ATPG vendors.

Not all "Commercial Off The Shelf" board suppliers will want to supply full proprietary design information for a third party to diagnose problems.

It will therefore be necessary to breakdown the diagnostic capability to 3 primary categories.

1. GO/NOGO Test
2. Device Pin Fault
3. Net and Pin Fault

Each of the above categories requires different levels of design information, varying from none to full net and component listings.



System JTAG a Motorola Perspective

SJTAG Diagnostic Requirements (Cont)

GO/NOGO

No design data needed just a test vector suite.

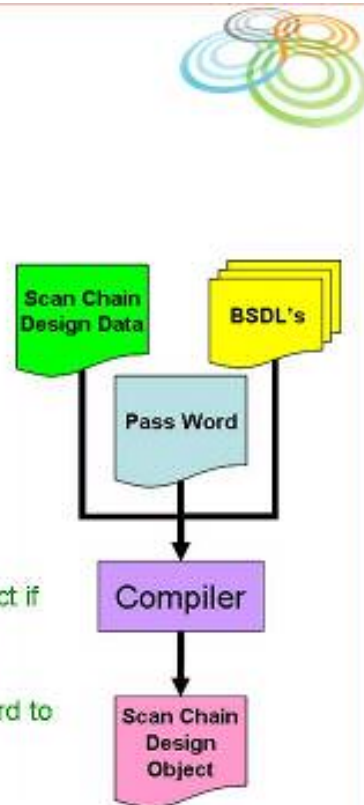


Device Pin Fault Diagnostic Reporting

To achieve this level of diagnostic only the UUT scan chain design and BSDL information is required. Ideally this scan chain description file should be compiled/compressed into a single scan chain design object which can be password protected.

Advantages:

- Small and compact could be embedded in product if required
- Hard to extract design interconnect information
- Remote diagnostic system has to supply password to access file.



System JTAG a Motorola Perspective

SJTAG Diagnostic Requirements (Cont)

Net & Pin Fault Reporting

To achieve this level of diagnostic full UUT net list and component data is required as well as the scan chain design and BSDL information.

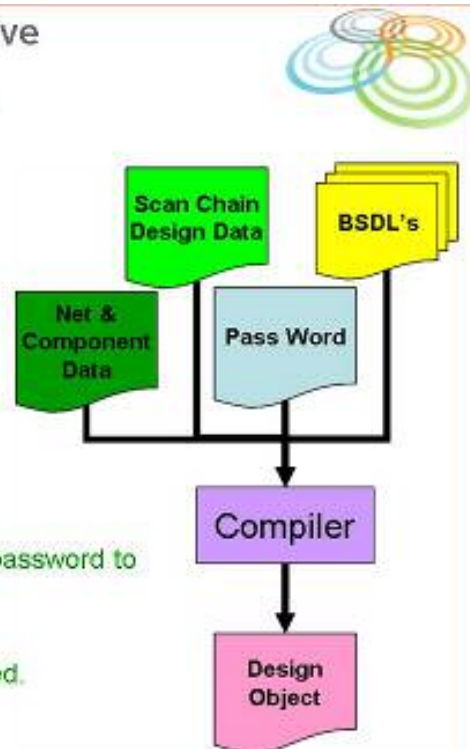
Ideally all the design data should be compiled/compressed into a single design object which can be password protected.

Advantages:

- Improved diagnostics.
- Remote diagnostic system has to supply password to access file.

Disadvantages:

- Design Object is large not easily embedded.
- Design data security risk.



System JTAG

SJTAG Design Data Requirements



Scan Chain Description File

There is a JEDEC standard for Scan Chain description.

(EIA/JESD32 Standard For Scan Chain Description)

<http://www.jedec.org/download/search/jesd32.pdf>

Can JESD32 be used?

- JESD32 does not support designs with multiple scan chains controlled via scan bridge type devices.
- JESD32 chain description format is complex for SJTAG requirements and is primarily targeted at programmable devices.

A new Scan Chain Description File (SCDF) is required that is simpler, smaller and secure.



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System JTAG



Example of a possible scan chain description file format

Concept:

The initial ASCII SCDF file would include:

- Generic design data
- A list of all BSDL files required for the design
- A description of any B-Scan chain control devices.
- Definition of each B-Scan chain within the design.

This would be compiled or compressed into a single pass word protected file. If required BSDL files could be excluded



```
[DESIGN_DATA]
  DESIGN_NAME    "Test_Board"
  DESIGN_NUMBER  "SVLN8634"
  DESIGN_REV     "01"
[END_DESIGN]

[BSDL_INCLUDE]
  BSDL_PATH "C:\scdf\scdf\" -- BSDL file default path
  INCLUDE "icmxof200e_fpga256.bsd" -- BSDL to be included in compressed object
  INCLUDE "xc4vtx40_f1148.bsd"
  INCLUDE "xc4vtx60_f1148.bsd"
  INCLUDE "MPC8541E.bsd"
  PATH "F8176.bsd" -- BSDL to be pulled from BSDL PATH not
  -- to be included in SCDF compressed object.

  INCLUDE "TMS320TC1100P620b.bsd"
[END_BSDL]

[ACCESS_DEFINITION]
  PRIMARY_0_JTS03 (TAP_0,TAP_1,CASCADE_0) "U30000"
  CASCADE_0_JTS03 (TAP_2, NONE, NONE) "U30001"
[END_ACCESS_DEFINITION]

[TAP_DEFINITION] -- Start of TAP definitions
  TAP_0 -- Define TAP 0
  "icmxof200e_fpga256.bsd" "U18000" -- TDI First device in chain
  "icmxof200e_fpga256.bsd" "U66003" --
  "xc4vtx40_f1148.bsd" "U61000" --
  "xc4vtx60_f1148.bsd" "U48000" -- TDO Last device in chain

  TAP_1 -- Define TAP 1
  "MPC8541E.bsd" "U10000" -- First device in chain
  "F8176.bsd" "U65004" -- TDO Last device in chain

  TAP_2 -- Define TAP 3
  "TMS320TC1100P.bsd" "U30000" -- TDI First Device in chain
  "TMS320TC1100P.bsd" "U38000" -- TDO Last device in chain
[END_TAP_DEFINITION]
```

System JTAG



SJTAG Design Data Requirements

Net & Component Description File

There are many different net and component list formats, which should SJTAG adopt?

At this stage it's not important to push and resolve this issue as the proprietary nature of such data causes much concerns and consternation within different groups.

Motorola has no strong leaning towards any one format, however the final design object should support :

- Modularity, so that sensitive elements can be excluded.
- The design object is as small as possible for possible embedding.
- That it's password protected for security.



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System JTAG



Standard Requirements Test Vector Description

STAPL (Standard Test and Programming Language) is currently seen as the main option for describing test vectors for the SJTAG environment, although a full review of features needs to be carried out.

STAPL

- Is targeted at IEEE1149.1 test & programming
- Has an ASCII & Binary format
- Has sufficient instructions for test sequencing and control
- APTG vendors are already familiar with the format
- Has an already established set of tools available from multiple sources not just APTG vendors
- Has support for embedded integration

There will no doubt be some modifications required to STAPL to achieve true SJTAG, but it's a good starting point.

Standard Requirements Test Vector Return Format

An area where additional work is required is the vector return format from STAPL due to the GOTO and LOOP constructs within the language.



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System JTAG



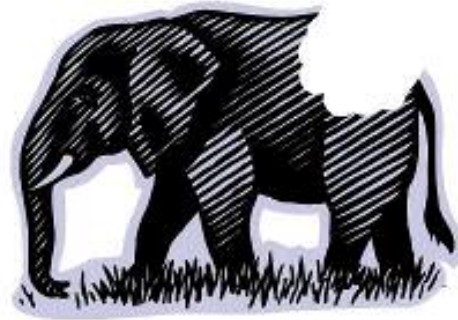
SJTAG IS A BIG PROBLEM

The industry must move forward now, we cannot wait for a fully ratified SJTAG specification this will take years.

SJTAG must breakdown the task into small manageable chunks.

First tackle

- Vector/Sequence definition
- Scan Chain definition
- Vector return definition
- Net and component list definition
- Physical Layer
- System configuration files
- System security
- SJTAG manager requirements

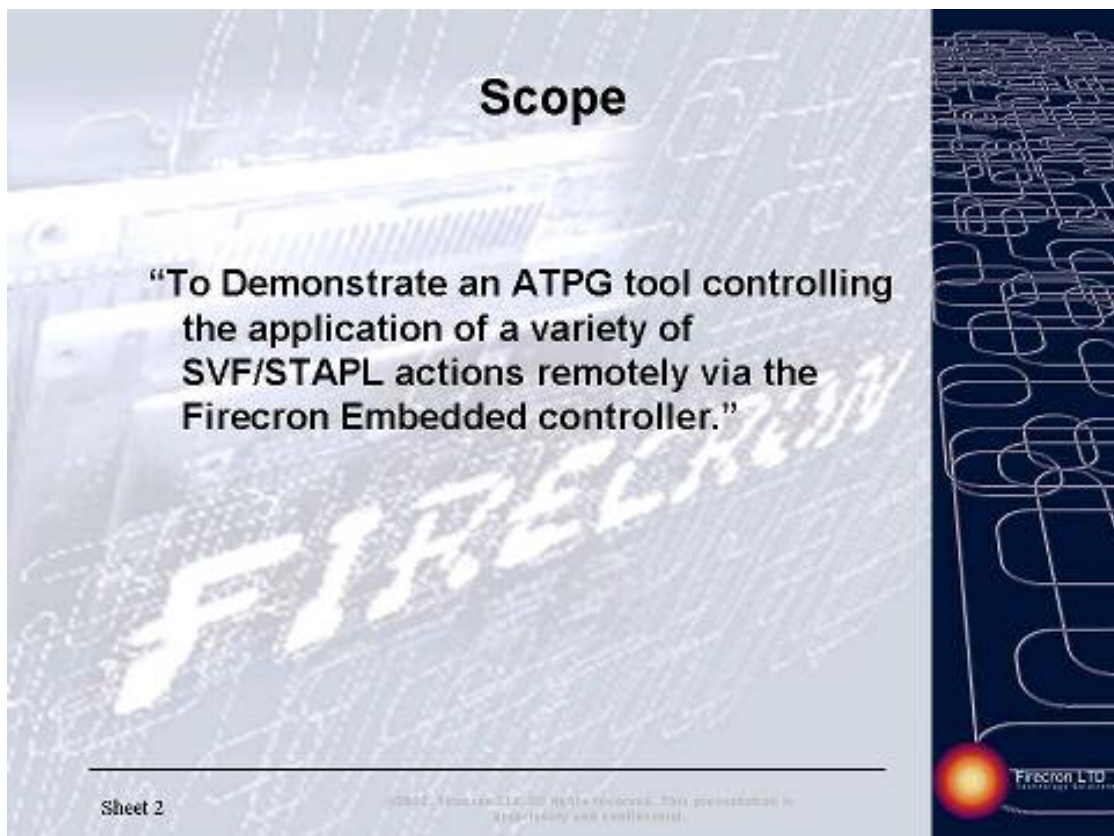
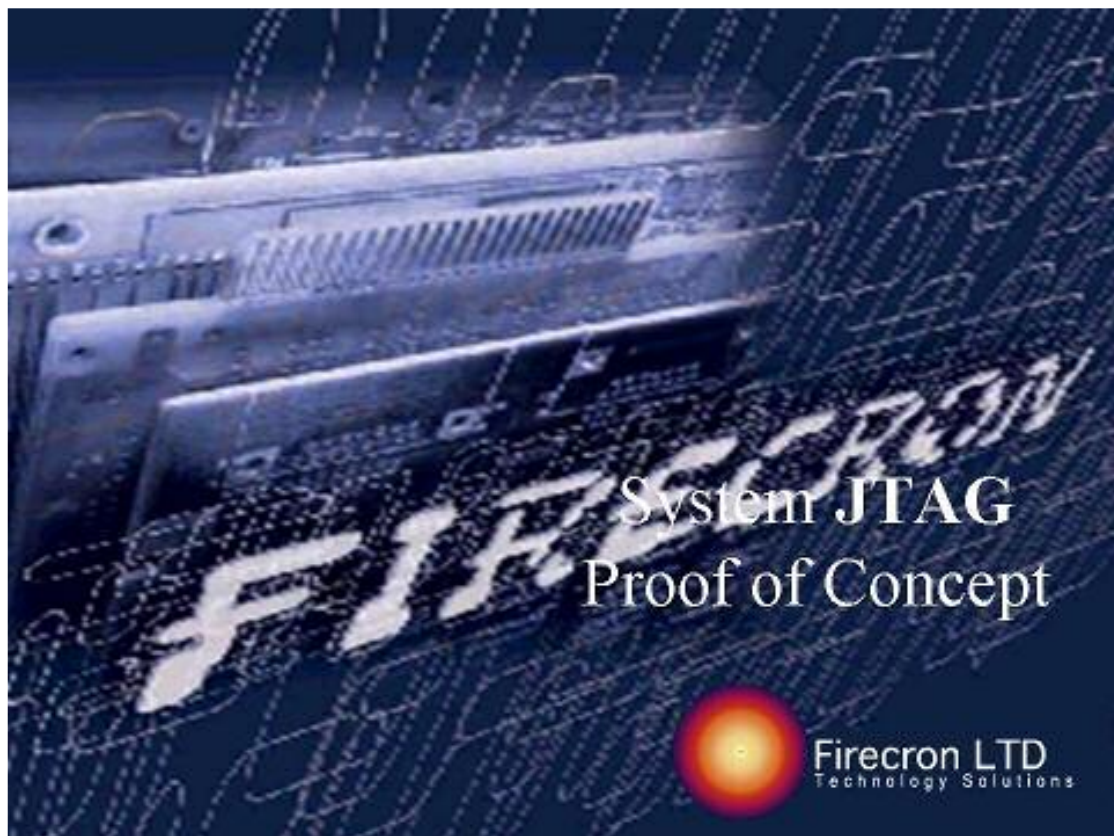


**How do you eat an Elephant ?
One BYTE at a time.**

15



EBTW'06 Presentation
Peter Horwood, Firecron



Objective

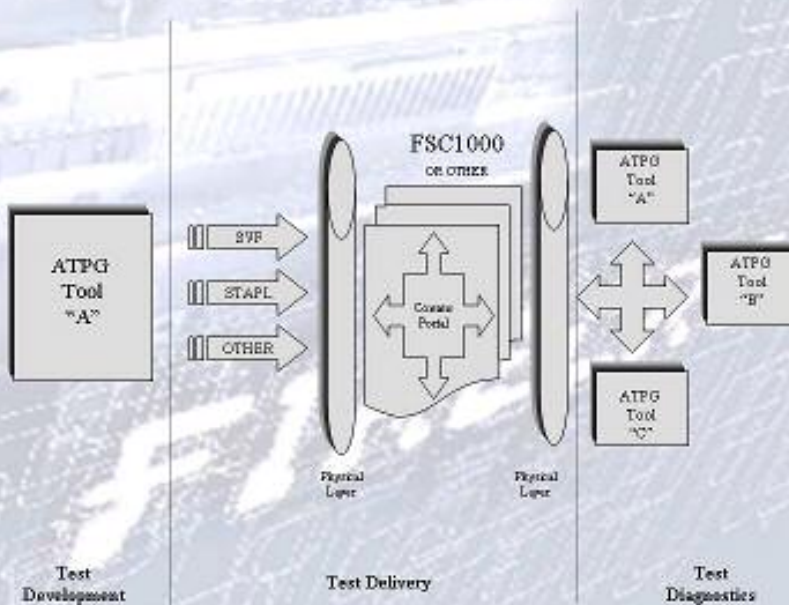
- Demonstration ATPG Tool boundary-scan system interacting with a Firecron embedded controller.
- Test vectors generated are downloaded with the Firecron embedded controller over an Ethernet connection.
- Diagnostic data is returned to the ATPG station for analysis.

Sheet 3

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SJTAG

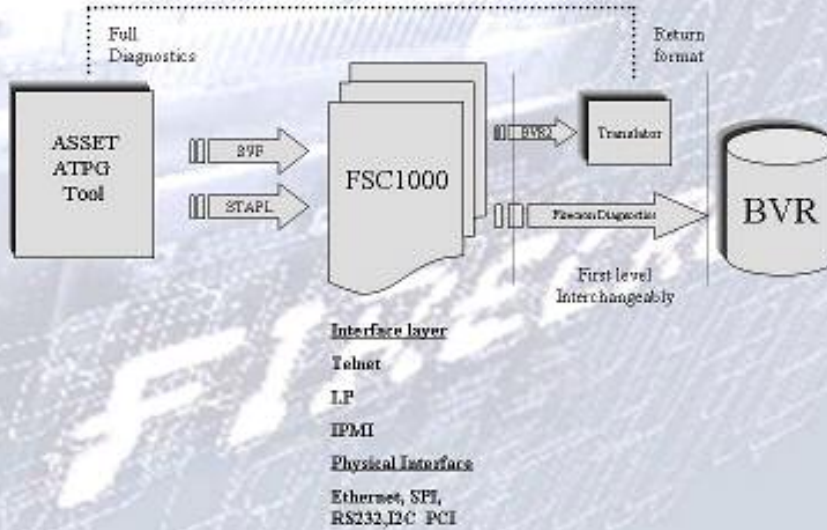


Sheet 4

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The Demo

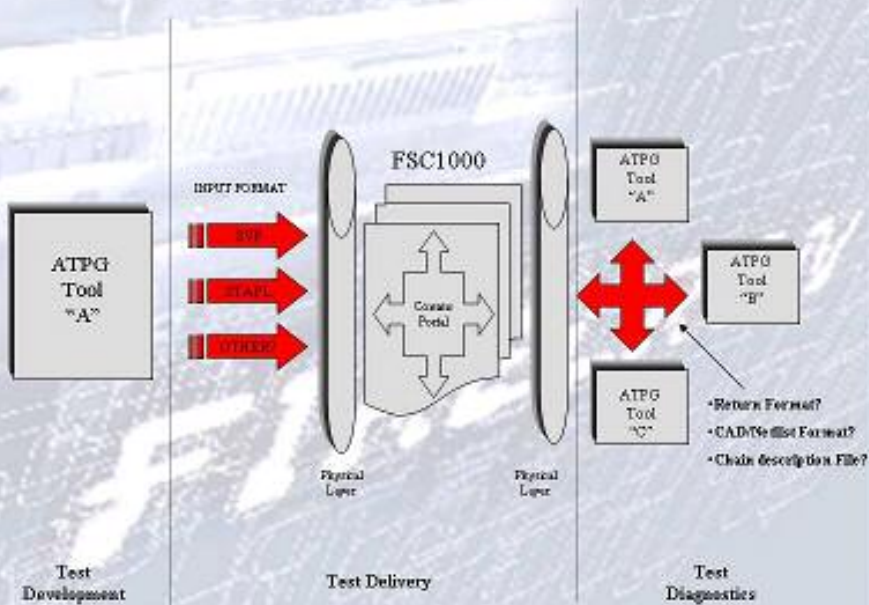


Sheet 5

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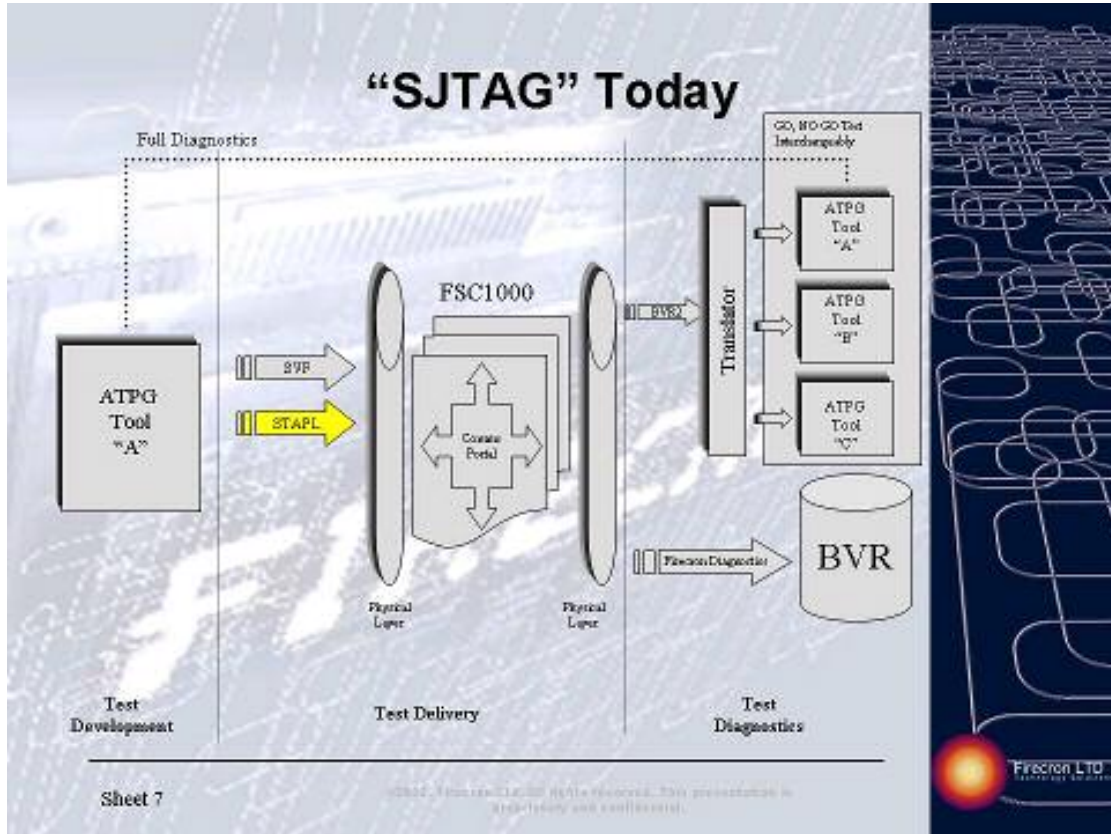
SJTAG Challenges



Sheet 6

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