



SJTAG Meeting at EBTW 2006

SJTAG Fringe Meeting at EBTW'06
Wednesday 24 May, 2005
1:00 PM – 3:45 PM
Tanners Room
Chilworth Manor, Southampton, UK

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EBTW 2006: Agenda

Ben Bennetts, SJTAG Chairman: Introduction/status of SJTAG.

Views from the industry

- Test manager vendors. Adam Ley, ASSET InterTech, USA
- Systems industry. Steve Harrison and Steve Lakin, Motorola, UK
- Scan support device vendors. Peter Horwood, Firecron, UK

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 **Who's in the Room?**

- Mick Austin, JTAG Technologies, FI
- Jan Heiber, Goepel, DE
- Erik Larsson, Linköpings Universitet, Sweden
- Ben Bennetts, Bennetts Associates (SJTAG Chairman), UK
- Steve Harrison, Motorola Networks, UK
- Bill Eklow, Cisco Systems, USA
- Peter Horwood, Firecron, UK
- Eugene Mullen, Firecron, UK
- Jim Webster, Consultant (ex-BAE Systems), UK
- Thomas Kronqvist, Saab Test Systems, SW
- Markku Moilanen, Oulu University, FI
- Adam Ley, ASSET InterTech, USA
- Artur Jutman, Technical University Tallinn, Estonia
- Anthony Sparks, JTAG Technologies, USA
- Jukka Antila, Nokia Networks, FI
- Bernard Sutton, Robot, UK
- Billy Fenton, International Test Technologies, IR
- Pete Collins, ASTER Ingenerie, FR
- James Stanbridge, JTAG Technologies, UK
- Chris Day, Abracad, UK
- Larry Osborn, ASSET InterTech
- Christophe Lotz, ASTER Ingenerie, FR
- Franc Novak, Josef Stefan inst., Slovenia
- Reg Waller, ASSET InterTech, UK
- Kevin Fotheringham, ASSET InterTech, UK
- Patrick Au, IBM, UK
- Gunnar Carlsson, Ericsson, Sweden
- Frans de Jong, Philips, NL
- Thomas Wenzel, Goepel Electronic, DE
- Ville Hassinen, Ericsson, Sweden
- Steve Okell, Tandberg TV, UK

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 **May 2006: SJTAG Initiative**



**System JTAG
Supporting eXternal and Embedded Boundary Scan Test
(XBST, EBST)**

Extracted from a white paper from the SJTAG group

Ben Bennetts, SJTAG Chairman

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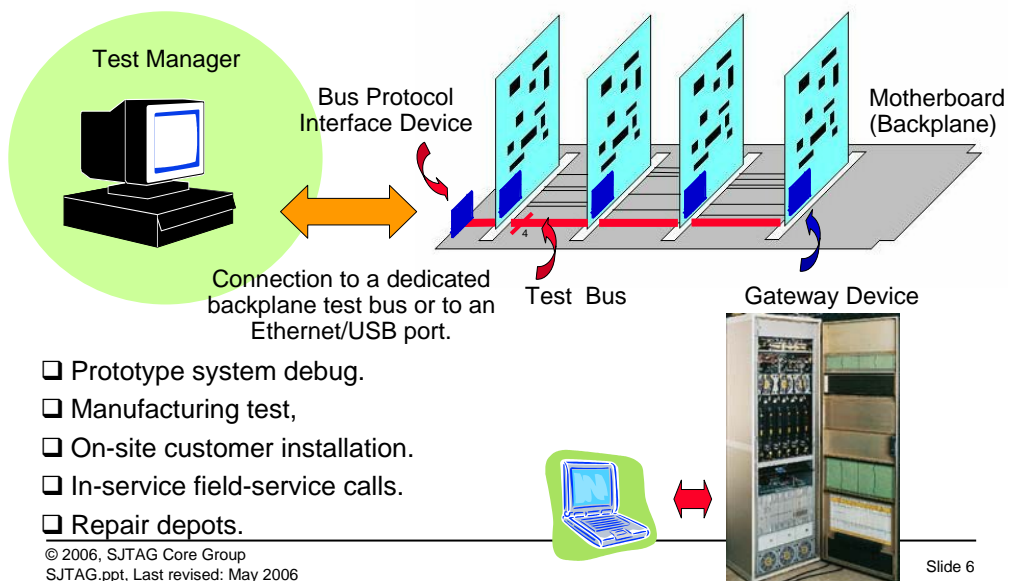
Background to SJTAG

- Kick-off meeting at the May 2005 European Board Test Workshop, Tallinn, Estonia: 14 attendees
- Representatives from ASSET InterTech, BAE Systems, Cisco, Ericsson, Firecron, Goepel, ITT, JTAG Technologies, National Semiconductor, Nokia, Saab Test + Independent Consultants
- Follow-on meetings at ITC 2005 and EBTW 2006
- Presentations available at www.dft.co.uk/SJTAG

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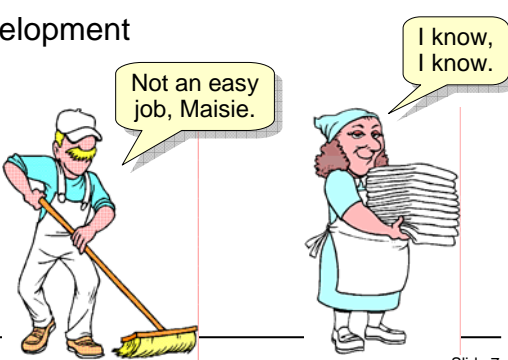
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What Are We Talking About?



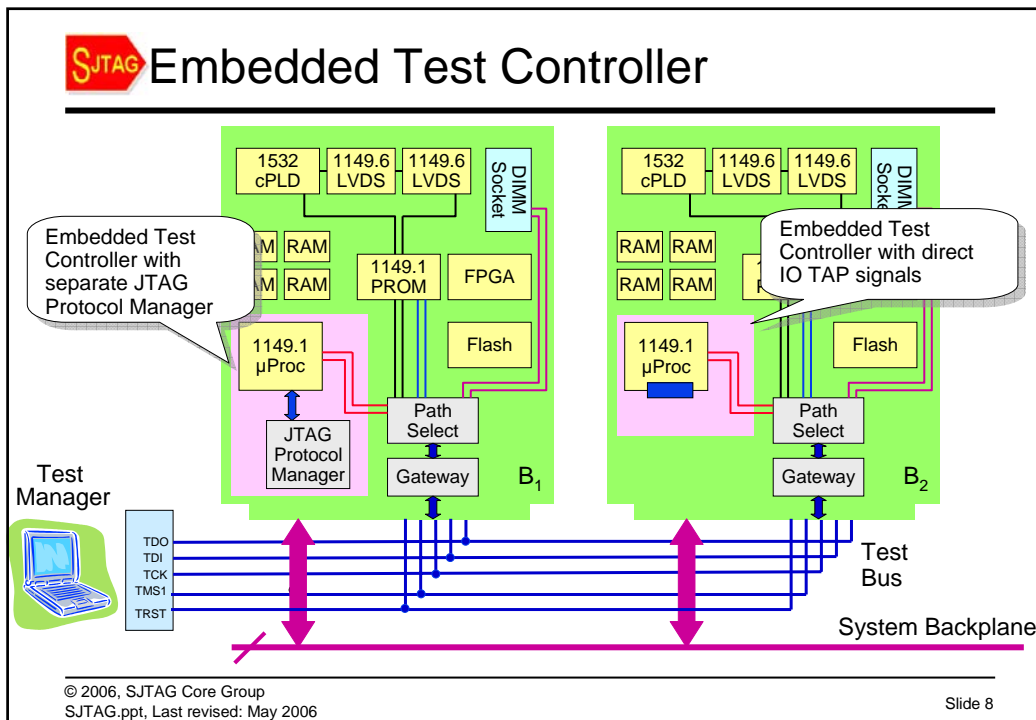
SJTAG We Are Still Defining Terms ..

- UUT
- System
- Test and Configuration
- eXternal Boundary Scan Test
- Embedded Boundary Scan Test
- Test Manager: program development and runtime controller
- Embedded Test Controller
- JTAG Protocol Manager
- Gateway Device



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SJTAG System Test Use Scenarios

The diagram illustrates the system test use scenarios. On the left, a **Test Manager** (represented by a computer icon) is connected via a double-headed orange arrow to a **Bus Protocol Interface Device**. This device is connected to a **Motherboard (Backplane)** which contains a **Test Bus** and a **Gateway Device**. A red arrow labeled '4' indicates the connection path from the interface device to the test bus. A blue arrow indicates the connection from the test bus to the gateway device.

Connection to a dedicated backplane test bus or to an Ethernet/USB port.

- Prototype system debug.
- Manufacturing test,
- On-site customer installation,
- In-service field-service calls.
- Repair depots.

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SJTAG eXternal Boundary Scan Test (XBST)

The diagram illustrates the eXternal Boundary Scan Test (XBST) setup. On the left, a **Test Manager** (represented by a computer icon) is connected via a double-headed orange arrow to a **Bus Protocol Interface Device**. This device is connected to a **Motherboard (Backplane)** which contains a **Test Bus** and a **Gateway Device**. A red arrow labeled '4' indicates the connection path from the interface device to the test bus. A blue arrow indicates the connection from the test bus to the gateway device.

Standard or Proprietary WAN Communication Protocol

Test Manager provides:

- Learning the configuration of the system: what UUTs are present, in what slots, etc
- Creating (off-line) and applying (on-line) an overall UUT and system test plan
- Response capture and analysis
- Overall control of all test and config operations

“Bare bones” implementation

- Backplane access (Ethernet, USB, etc)
- UUT addressing scheme for multi-drop e.g. a gateway device.

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SJTAG Embedded Boundary Scan Test (EBST)

Test Manager provides:

- Overall control of embedded test and configuration sequences: data load, start, results capture, logging, analysis and display

“Fully-loaded” implementation

- Backplane access (Ethernet, USB, etc)
- UUT addressing scheme for multi-drop e.g. a gateway device
- Embedded Test Controller with or without a separate JTAG Protocol Manager
- On-board path selection, if required.

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SJTAG The Questions

Question: should I have an external Test Manager do all the work and just have “bare-bones” additions to the system, or should I have a “fully-loaded” Embedded Test Controller system and just use the Test Manager as an overall test runtime and configuration controller?


And, whichever way I go, what are the implications: tradeoffs, benefits, ability to leverage what already exists, invocation procedures, data formats and languages, etc.?

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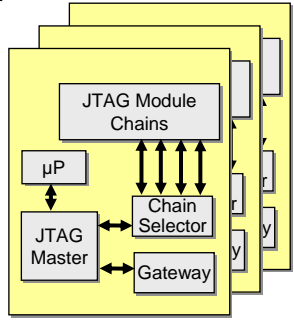


The Goal of SJTAG - 1



Test Manager
(External or Embedded)


- ❑ Vector and configuration data
- ❑ Response data
- ❑ Log and status data
- ❑ Commands
 - Vector management
 - Execution conditions set-up
 - Execution control
 - Response data retrieval
 - Log and status data retrieval
 - UUT recovery from a test




Multi-Board System

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The Goal of SJTAG - 2



The goal for SJTAG is:

for all variants of XBST and EBST, to define the data contents and formats communicated:

between external Test Manager platforms and internal Embedded Test Controllers, and

between Embedded Test Controllers and the UUTs they serve

in an open-standard vendor-independent and non-proprietary way.

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The SJTAG Players

Scan Support
Device Vendors
Firecron
NatSemi
Texas Inst
Etc



Test Manager
Vendors
ASSET
Goepel
JTAG Tech
Etc



To Become Involved in SJTAG ...

Send e-mail to Ben Bennetts at ben@dft.co.uk



Reminder: go to

www.dft.co.uk/SJTAG

to download the current version
of the white paper.

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