ITC 2006 Tutorial #8

Designing Testable Multi-Board Systems using 1149.1 Architectures: SJTAG

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Disclaimer

- This presentation is a personal view of what is happening within the SJTAG initiative. It is not an SJTAG-endorsed presentation. Other members of SJTAG may have a different view of the objectives and status of SJTAG. This is the nature of formative activities.

Background to SJTAG

- Kick-off meeting at the May 2005 European Board Test Workshop, Tallinn, Estonia: 14 attendees
- Representatives from ASSET InterTech, BAE Systems, Cisco, Ericsson, Firecron, Goepel, ITT, JTAG Technologies, National Semiconductor, Nokia, Saab Test + Independent Consultants
- Follow-on meetings at ITC 2005, EBTW 2006, BTW 2006 and ITC 2006 (later this week)
- Presentations available at **www.dft.co.uk/SJTAG**

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Purpose of the Tallinn Meeting (1)

- Several systems companies are proposing or are already building quite sophisticated approaches to system level test based on the use of a suitable backplane test bus, such as 1149.1 or an alternative e.g. I^2C.
- The assumption is made that the boards already contain boundary-scan chains and that some form of multi-drop architecture allows access to individual boards and even individual devices on a board for test application (re-use of single-board tests or board-to-board tests) or in-system configuration/reconfiguration of on-board PLDs.
- Such techniques support various field service requirements and can be managed remotely (over a wireless network) or locally (over a wired connection) or be fully embedded.

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Purpose of the Tallinn Meeting (2)

- The field-service Development and Diagnostic Test Manager can be a free-standing system based on an extension to existing PC-based single-board boundary-scan testers.
- The question has arisen - is there a suitable JTAG Test Command and Data Language (TCDL) capable of covering the following basic requirements:
  - **Represent** embedded test data (e.g. vectors) efficiently
  - **Write** to, **Read** from and **Manage** test data stored on the board
  - **Run** an embedded test
  - **Configure** and **Validate** an on-board PLD
  - **Capture** the result of the test and **Compare** with the expected result
  - **Log** test execution details (time, date, result, etc)
  - **Send** specific test reports and service logs to the Test Manager.

Jump

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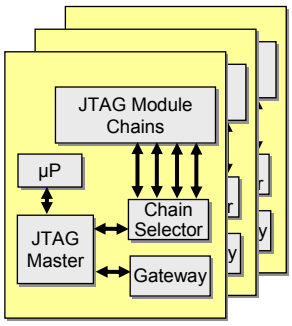
The Goal of SJTAG - 1

Test Manager
(External or Embedded)

- Vector and configuration data
- Response data
- Log and status data
- Commands
  - Vector management
  - Execution conditions set-up
  - Execution control
  - Response data retrieval
  - Log and status data retrieval
  - UUT recovery from a test



Multi-Board System

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The Goal of SJTAG - 2

The goal for SJTAG is:

for all variants of XBST and EBST, to define the data contents and formats communicated:

between external Test Manager platforms and internal Embedded Test Controllers,

and

between Embedded Test Controllers and the UUTs they serve

in an open-standard vendor-independent and non-proprietary way.

Targets and Focus (10 Nov 05 ITC Meeting)

- Four main industries
  - Telecoms
  - Server/mass storage
  - Mil/Aero
  - Automotive
- Need ways of describing:
  - The nature of the Test Manager function: all external, all embedded, distributed
  - The access and communication protocols
  - Test flow control and data requirements for test, debug, diagnosis, configuration, etc
- Issues:
  - Security
- Initial focus: telecoms, especially MicroTCA/ATCA but not exclusively.

Core Group (September 2006)

Change of Leadership

SJTAG Core Group
Brad Van Treuren, Lucent Technologies – Chair
Gunnar Carlsson, Ericsson – Vice Chair
Ben Bennetts, Bennetts Associates – Chair Emeritus
Anthony Sparks, JTAG Technologies
Bill Eklow, Cisco Systems
Ken Filliter, National Semiconductor
Steve Harrison, Motorola Networks
Peter Horwood, Firecron
Jim Webster, BAE Systems
Adam Ley, ASSET InterTech

Scan Support Device Vendors
Test Manager Vendors
System Company End Users

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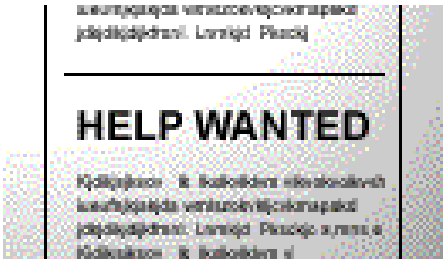
Where Are We Now?

- We are defining:
  - Demos.
  - Use scenarios.
  - University projects
- We are also looking for more volunteers to become active in the future (more later)



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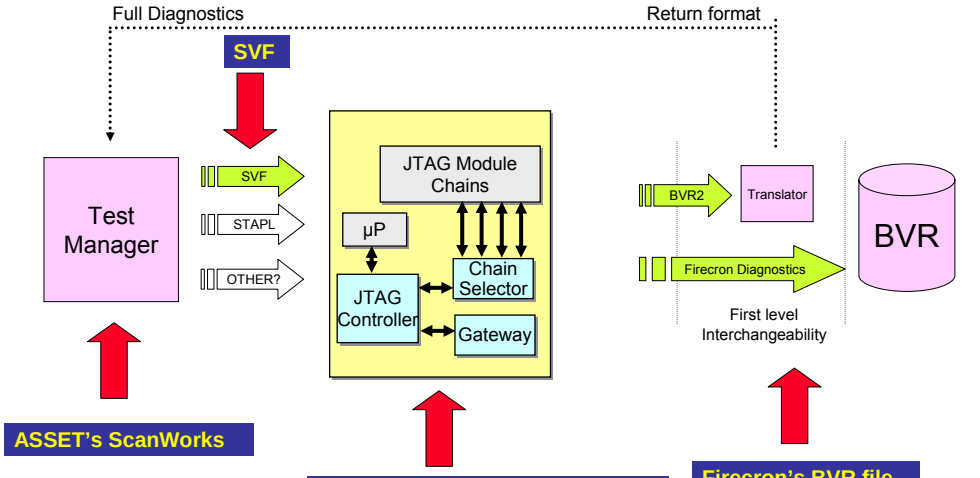
Demo 1: Shown at EBTW May 2006



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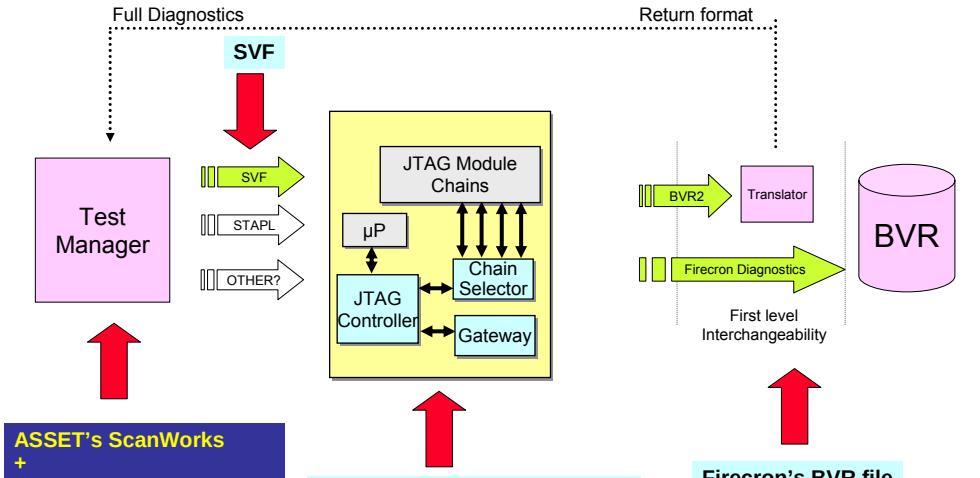
Building the Demos: Test Manager



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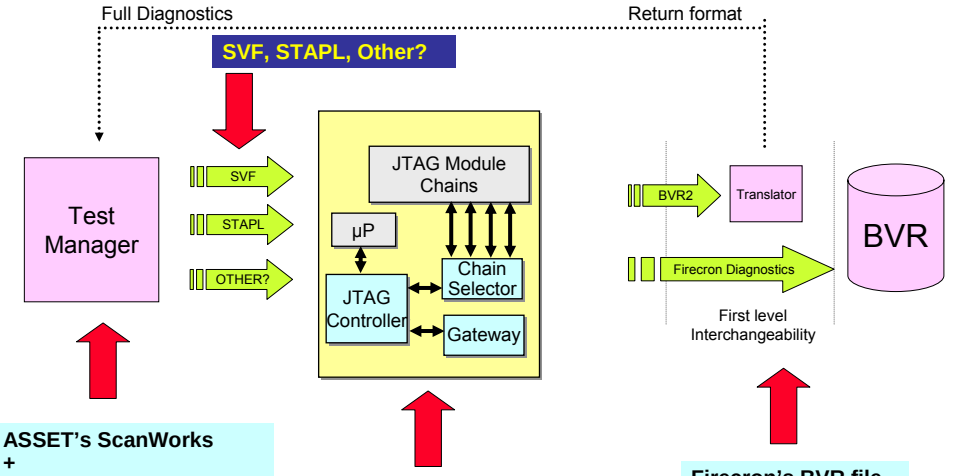
Building the Demos: Input Language



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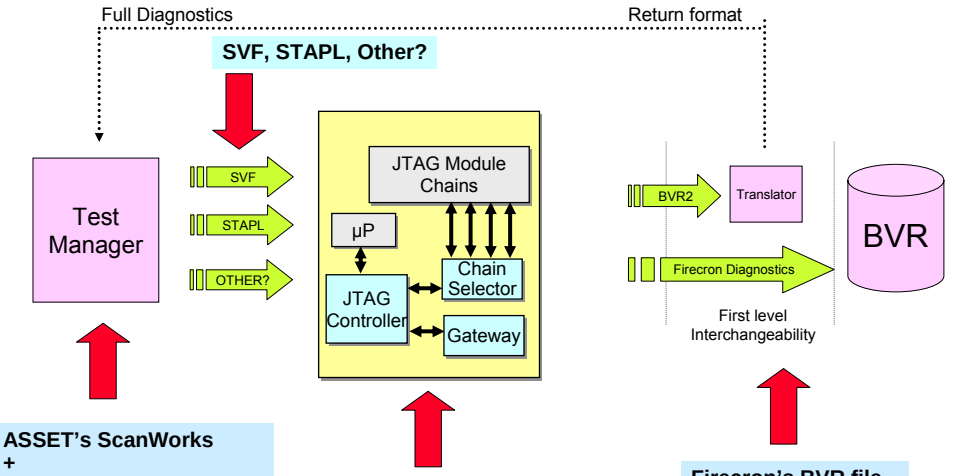
Building the Demos: JTAG Controller



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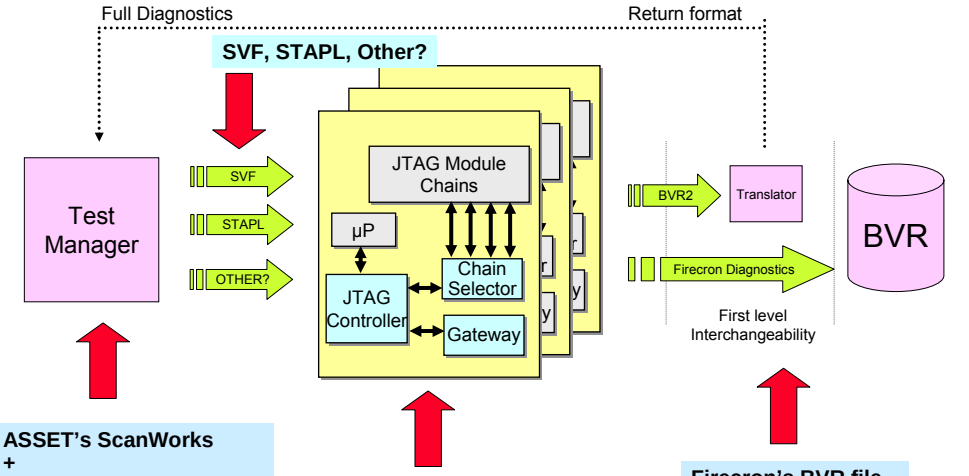
Building the Demos: Multiple Boards



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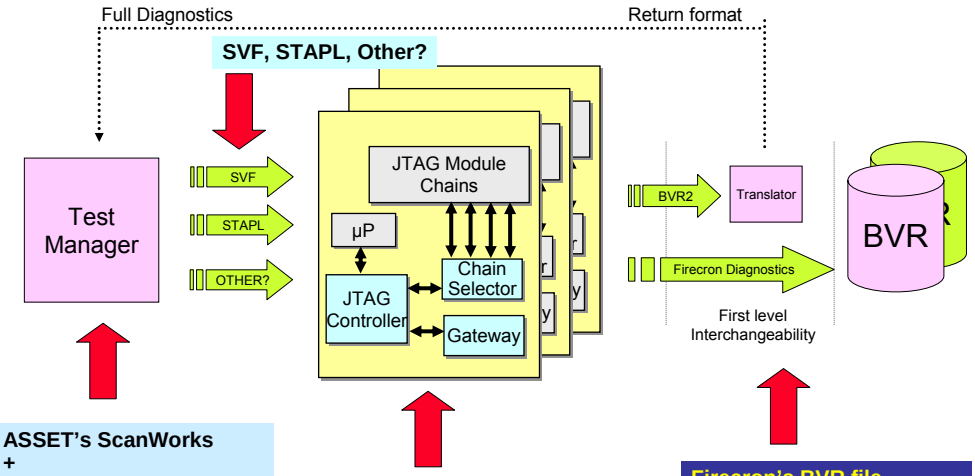
Building the Demos: Return Format



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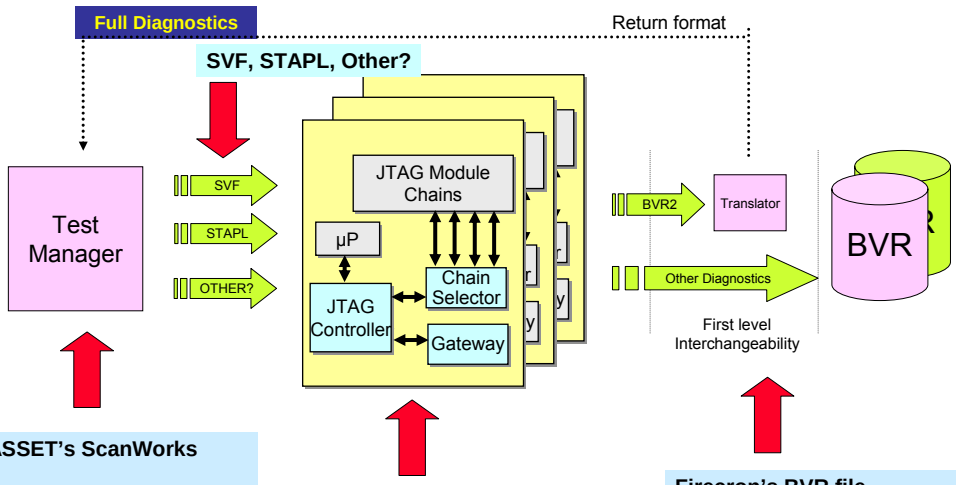
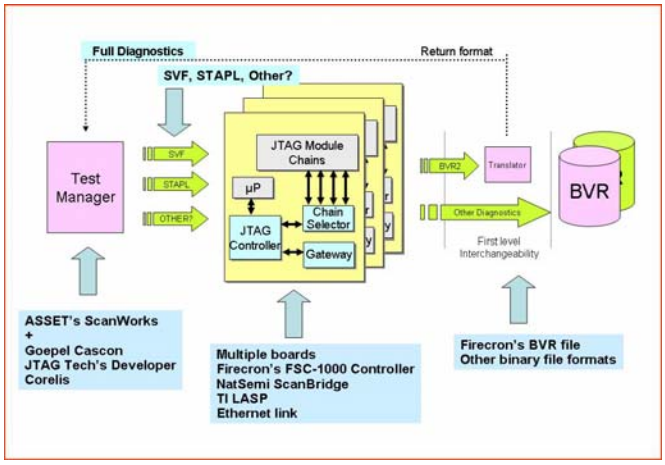
Building the Demos: Diagnostics



Adding Use Scenario Considerations



- ❑ Prototype system debug.
- ❑ Manufacturing test,
- ❑ On-site customer installation.
- ❑ In-service field-service calls.
- ❑ Repair depots

What's Next?

- SJTAG open meeting this week
  - Thursday, October 26, 10:30 – 12:30, Room 202
- To join SJTAG's extended group: e-mail awareness of future events, access to archived and new documents:
  - Send e-mail to Brad Van Treuren, **vantreuren@lucent.com**

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State of the SJTAG Initiative

ITC 2006 Meeting

Bradford G. Van Treuren
Chairman

SJTAG

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Direction of the SJTAG Initiative

- My first attempt at the Scope – Not an official statement
- This standard will develop a methodology for access to test, debug, instrument, and emulation features (but not the features themselves) of devices via the IEEE 1149.1 Test Access Port (TAP) for the board and system (multiple board) domains. The elements for this methodology include a description language describing the structure of the IEEE 1149.1 connections in the system; a description of data representation formats for test vectors, diagnostic analysis, and data logging; and software application programming interfaces (APIs) defining command primitives facilitating communications between functional command, control, and data modules of a Test Manager application.

➢Do not use this draft as fact!

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Direction of the SJTAG Initiative

- My first attempt at the Purpose – Not an official statement
- There is currently no defined, independent standard for this test technology. Each vendor is free in the way of implementing test hardware and software functionality on their boards. Without an independent standard, testability at the system level is reduced or impossible making the test technology in the system less useful for users integrating designs from multiple sources – limiting the ability to use the test technology in other facets of a product's life cycle beyond manufacturing. In practice, the software used to perform test actions is written in an ad-hoc manner across the industry to access the IEEE 1149.1 features of the devices installed on the various boards of a system. Further, communications between remote and embedded hosts managing the tests applied to the system under test is non-existent or implemented using ad-hoc communications protocols. The purpose of the SJTAG initiative is to provide an extension of the IEEE 1149.1 standard specifically aimed at the configuration, control, management, and representation of the communications required at the hierarchical system and board level to perform operations on the IEEE 1149.1 Test Access Port (TAP) Controller of one or more devices, including multiple core devices, in a uniform way across all system modules.

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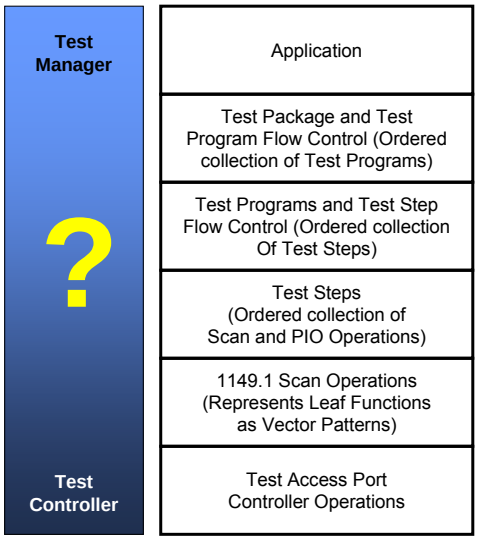
Layers of the Software for Traditional EBST



- Apply a set of vectors
- Capture a set of responses
- Compare responses to known expected values
- Conditionally apply next set of vectors based on response result of PASS or FAIL

➢ Fixed set of tests that are applied over and over again

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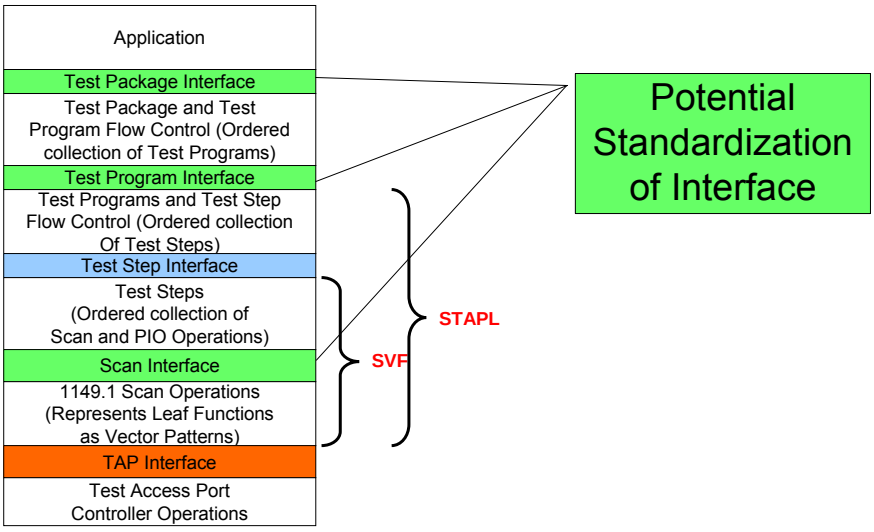
Interface Boundaries of the Software



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IJTAG Relationship with SJTAG

- IJTAG provides an interface bridge for a device package between embedded instruments and the external JTAG port of the device package
- IJTAG is an extension of the IEEE 1149.1 standard aimed at using the TAP to manage the configuration, operation, and collection of data from embedded instrumentation circuitry inside a device package
- IJTAG defines the data file format necessary to describe the instrumentation configuration, operation, and data registers that are accessible from the TAP for tools to generate commands for the instrument (i.e., BSDL for instruments)

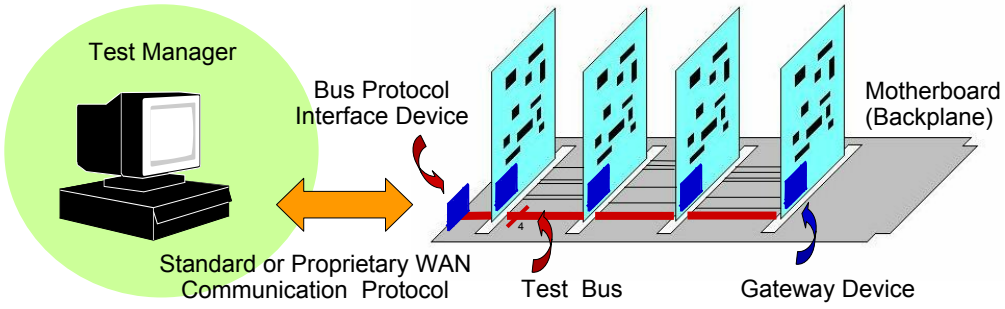
SJTAG Relationship with IJTAG

- SJTAG defines an interface methodology from external or embedded test systems to boards/blades installed in a system
- SJTAG defines an interface methodology from embedded test systems on boards to the device packages located locally on the board or daughter boards
- SJTAG defines an interface methodology from external or embedded test systems to the device packages located in system (The IJTAG world)

SJTAG Relationship with IJTAG

- SJTAG defines the software interfaces between layers of the interface methodology
- SJTAG defines the data description formats that describe the JTAG interface definition for each IEEE 1149.1 architectural module in the system

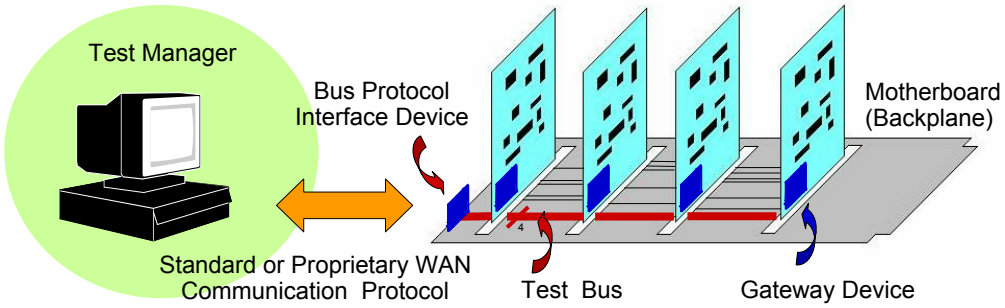
eXternal Boundary Scan Test (XBST)



Test Manager provides:
- ❑ Learning the configuration of the system: what UUTs are present, in what slots, etc
- ❑ Creating (off-line) and applying (on-line) an overall UUT and system test plan
- ❑ Response capture and analysis
- ❑ Overall control of all test and config operations

"Bare bones" implementation
- ❑ Backplane access (Ethernet, USB, etc)
- ❑ UUT addressing scheme e.g. a gateway device.

Embedded Boundary Scan Test (EBST)



Test Manager provides:
- ❑ Overall control of embedded test and configuration sequences: data load, start, results capture, logging, analysis and display

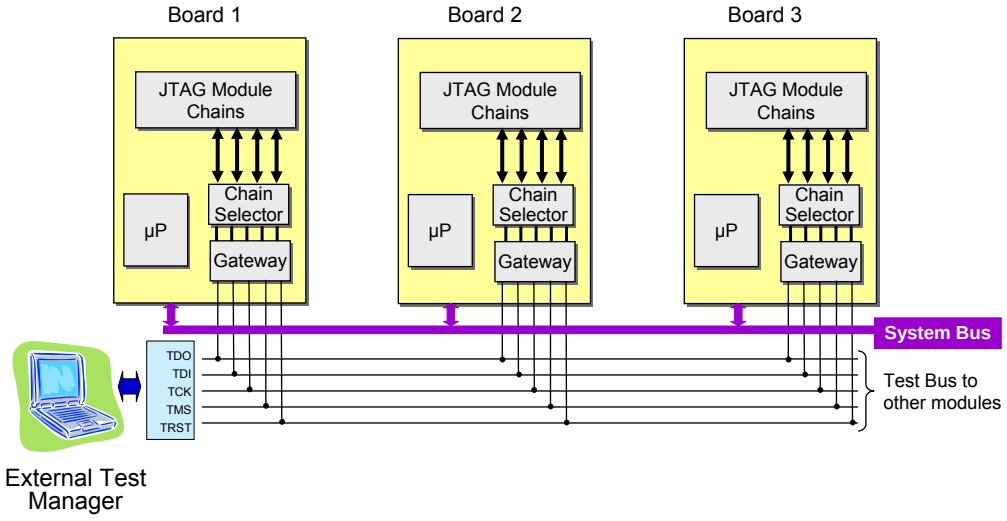
"Fully-loaded" implementation
- ❑ Backplane access (Ethernet, USB, etc)
- ❑ UUT addressing scheme e.g. a gateway device
- ❑ Embedded Test Controller with or without a separate JTAG Protocol Manager
- ❑ On-board path selection, if required.

System Level Test Architectures

- There are at least four major system level options:
  - All Slaves with a Backplane: **eXternal Boundary Scan Test (XBST)**
  - Single Master with a Backplane
  - Multiple Masters with a Backplane
  - Multiple Masters without a Backplane

Variants of **Embedded Boundary Scan Test (EBST)**

No Master – All Slaves (XBST)



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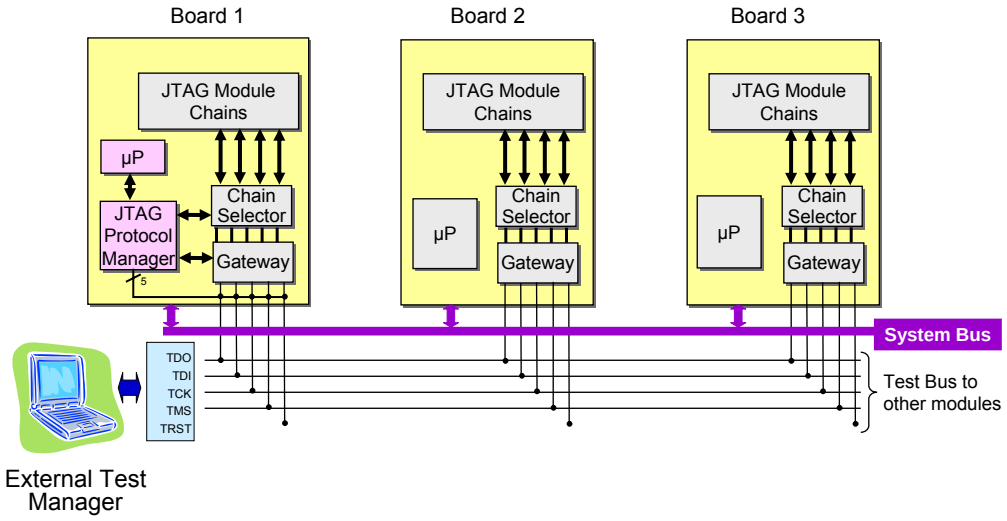
Single Master – Multiple Slaves (EBST)



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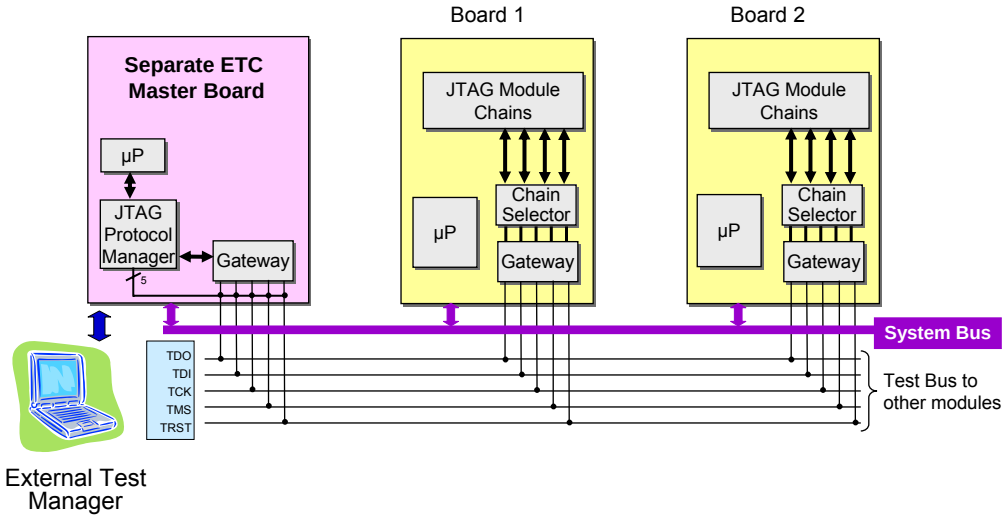
Single Master – Multiple Slave: Variant 1



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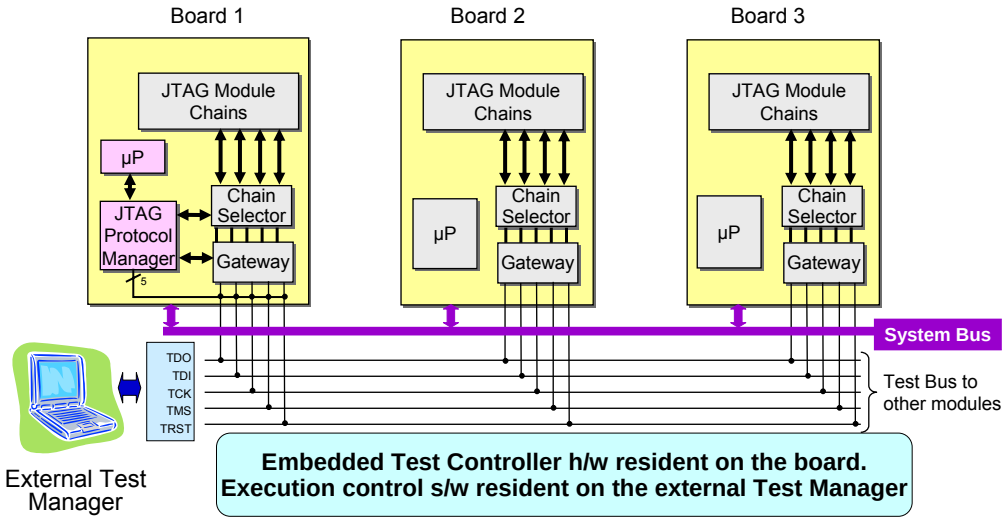
Single Master – Multiple Slave: Variant 2



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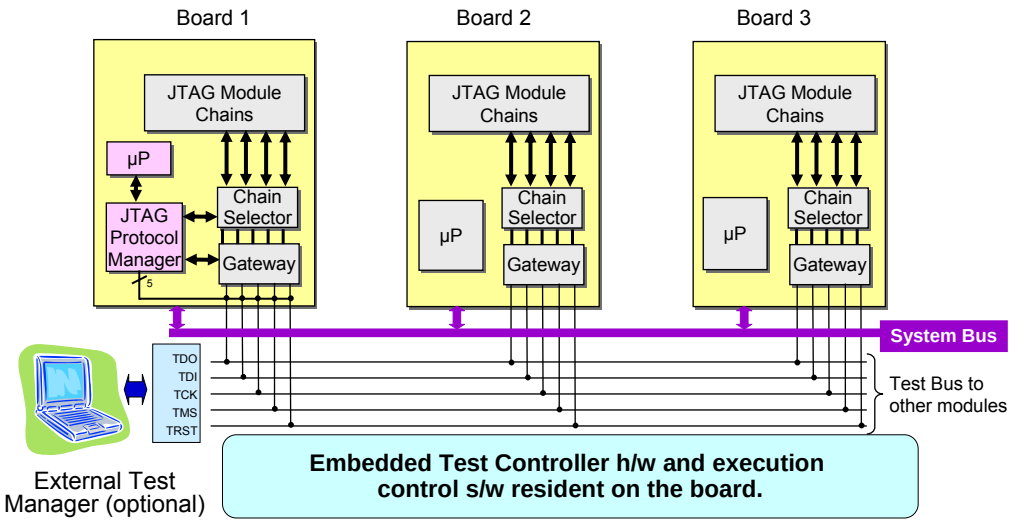
Single Master – Multiple Slave: Variant 3



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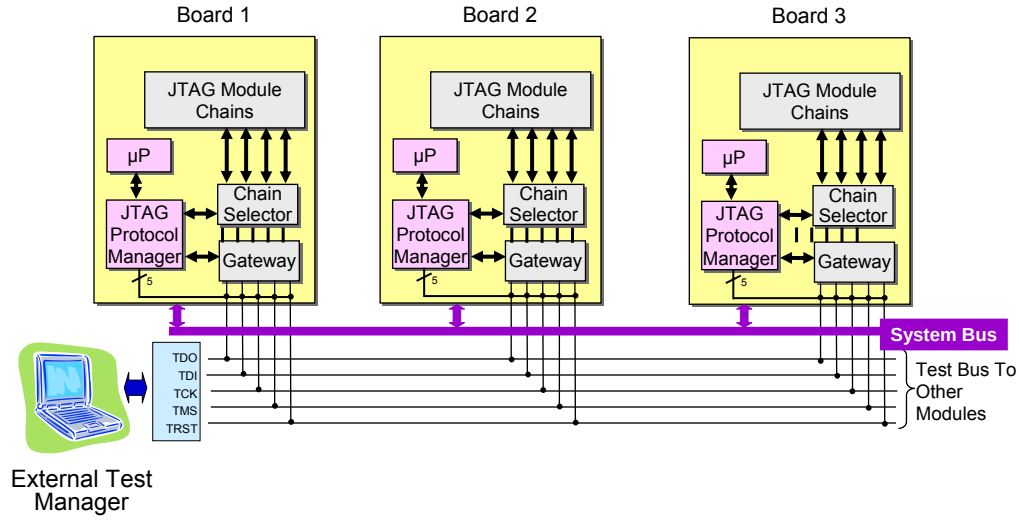
Multiple Masters with a Test Bus (EBST)



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