SJTAG in RBS at Ericsson

November 15, 2006

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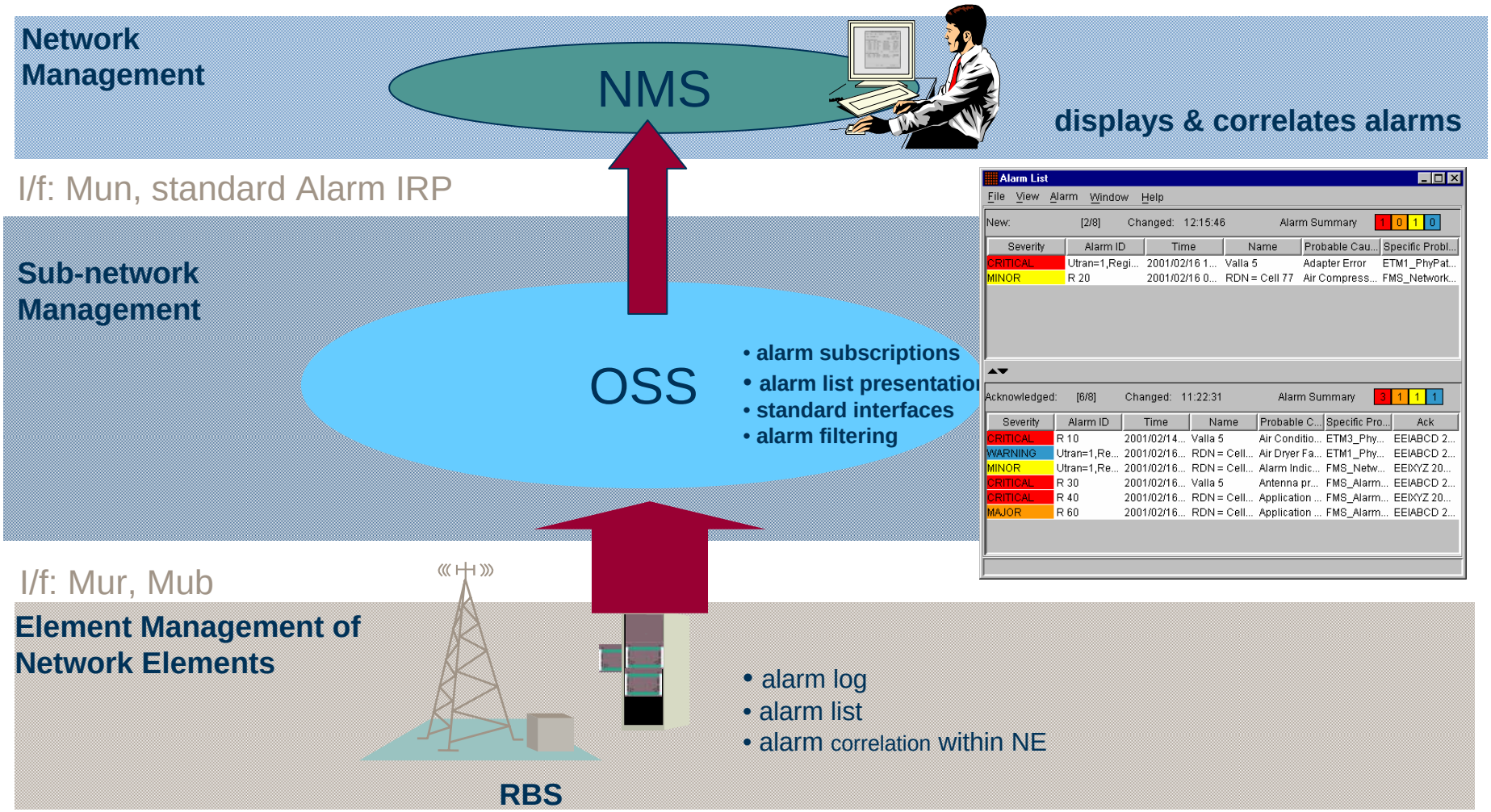
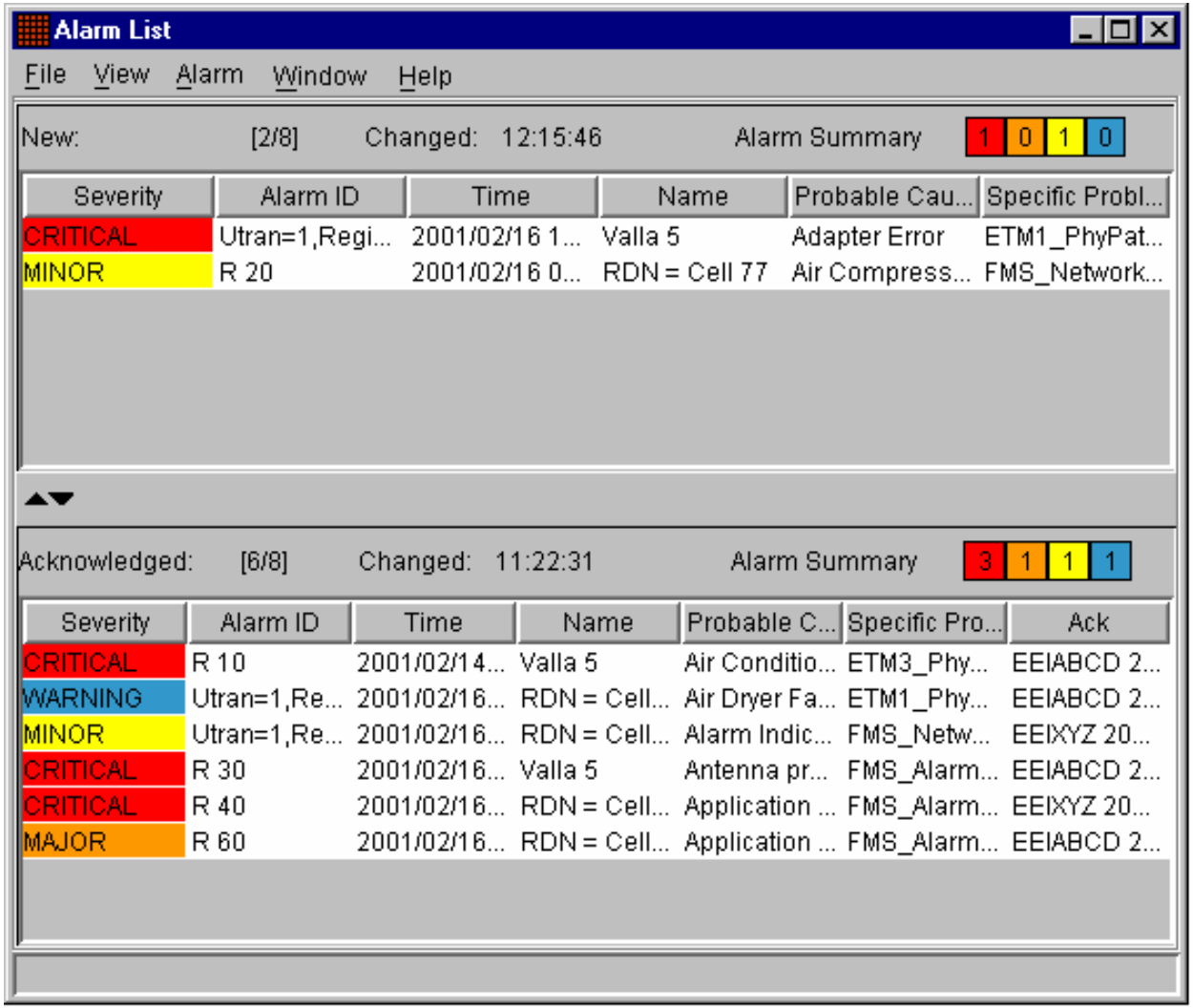
A Network Management View



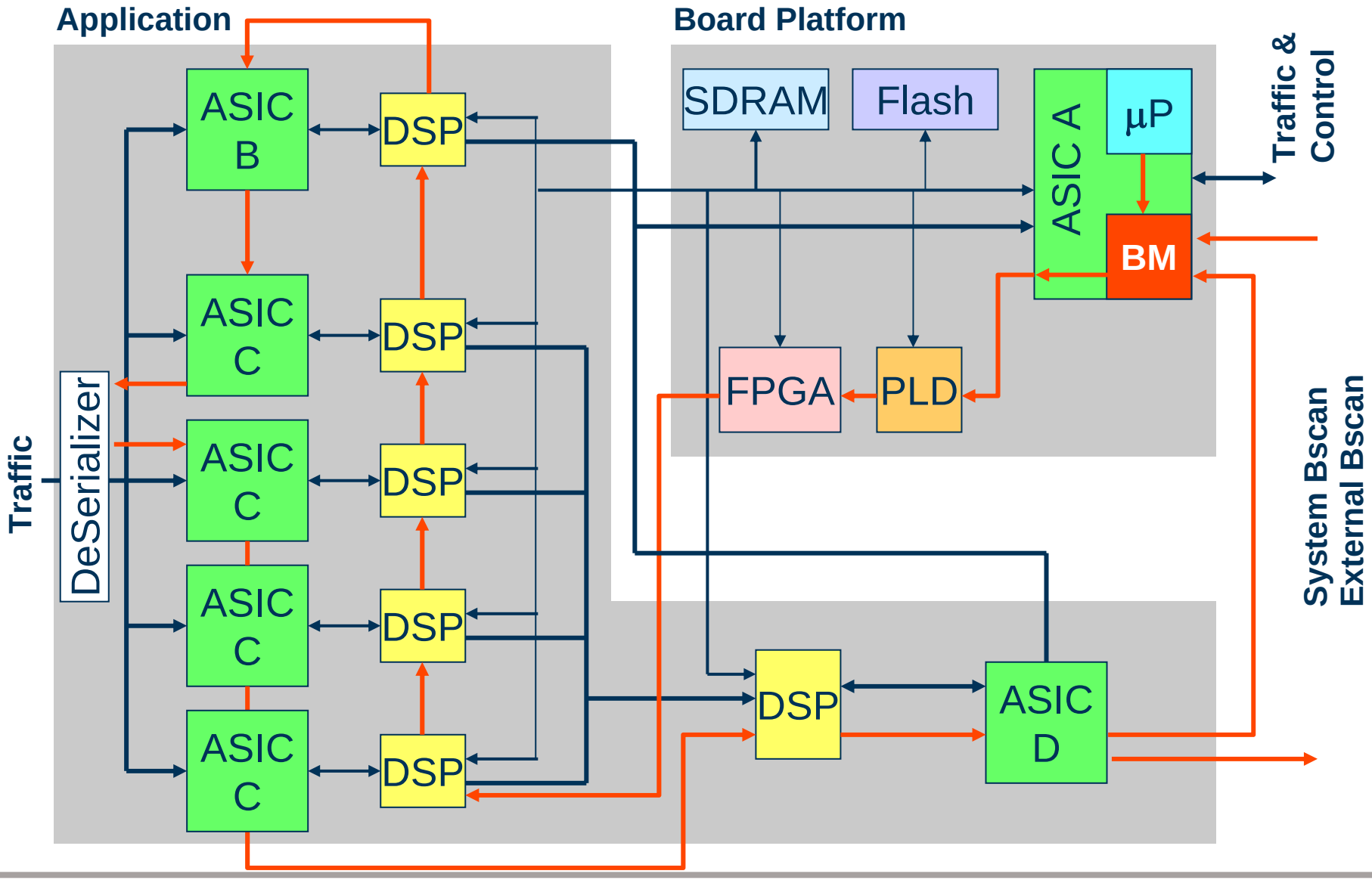
Alarm Display



EBST – Usage and Requirements

- Field test purposes
  - Validate HW fault related alarms, pinpoint replaceable unit
  - Detect latent faults at (re)start of boards or at regular tests
- Bscan test in the field
  - BScan is part of embedded test SW
  - Trade-off between test time and coverage
  - Diagnosis down to replaceable unit often sufficient
- In-system diagnostic test
  - Used at repair centers
  - Requires better coverage and diagnostic resolution
  - Not time critical

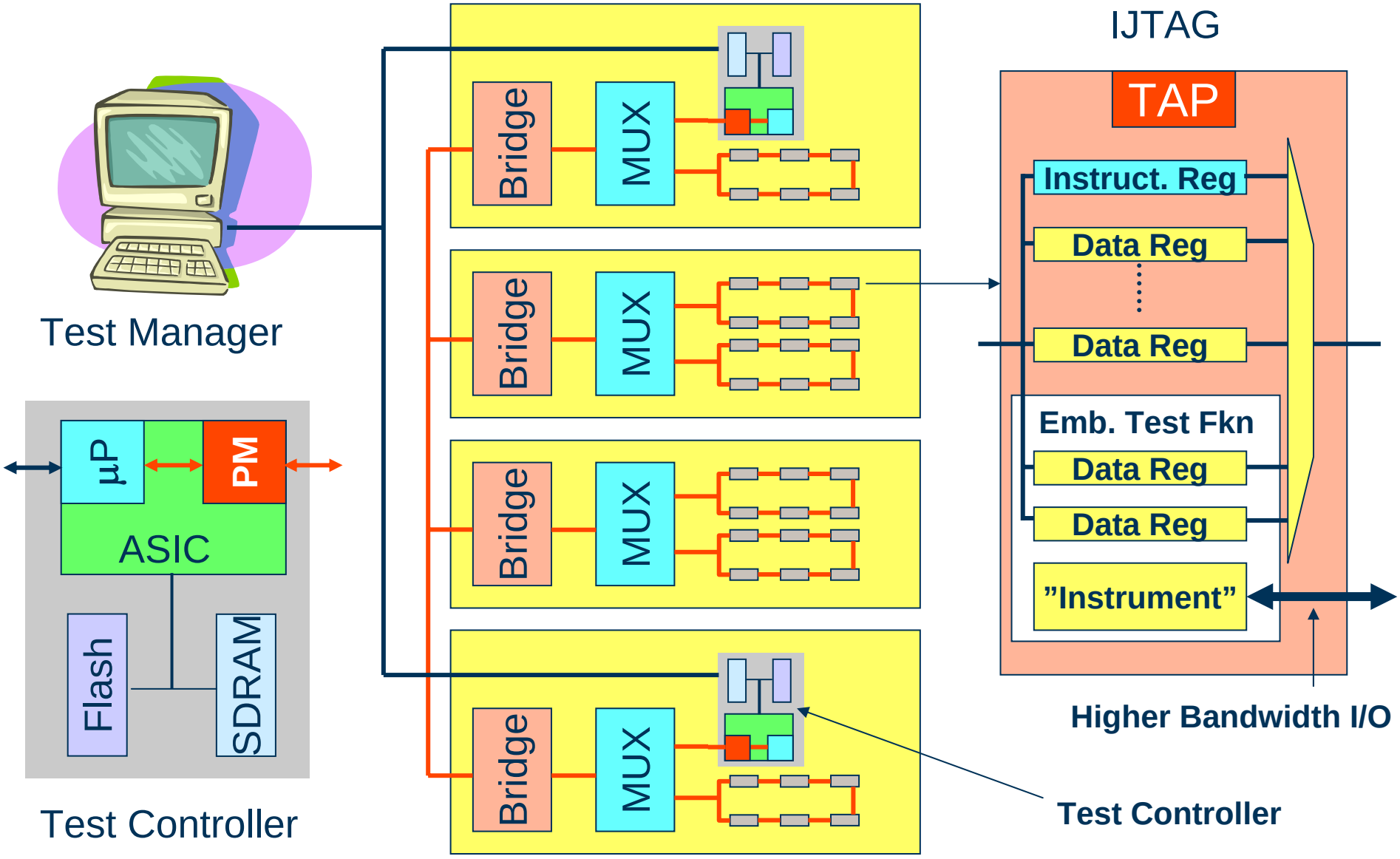
Embedded Boundary Scan Test



Typical EBST Operations

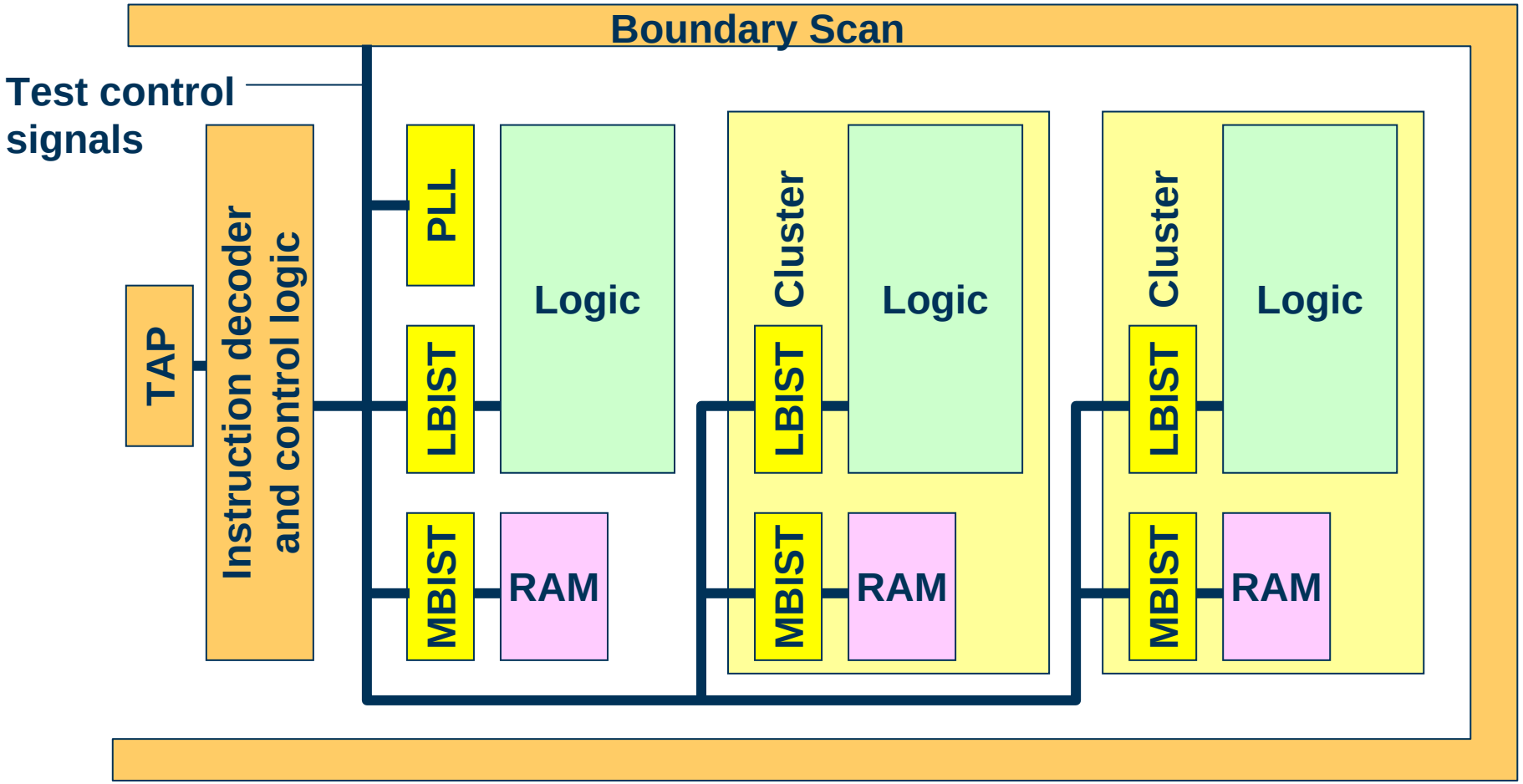
- Conventional (single board) interconnect test
  - Supported by SVF/STAPL standard languages
- In-system programming
  - Supported by STAPL
- System interconnect test using chain configuration devices (bridges, scan routers)
- Simple IJTAG operations (single board, no hierarchy)
- Complex IJTAG operations (through system and device hierarchies)

SJTAG and IJTAG

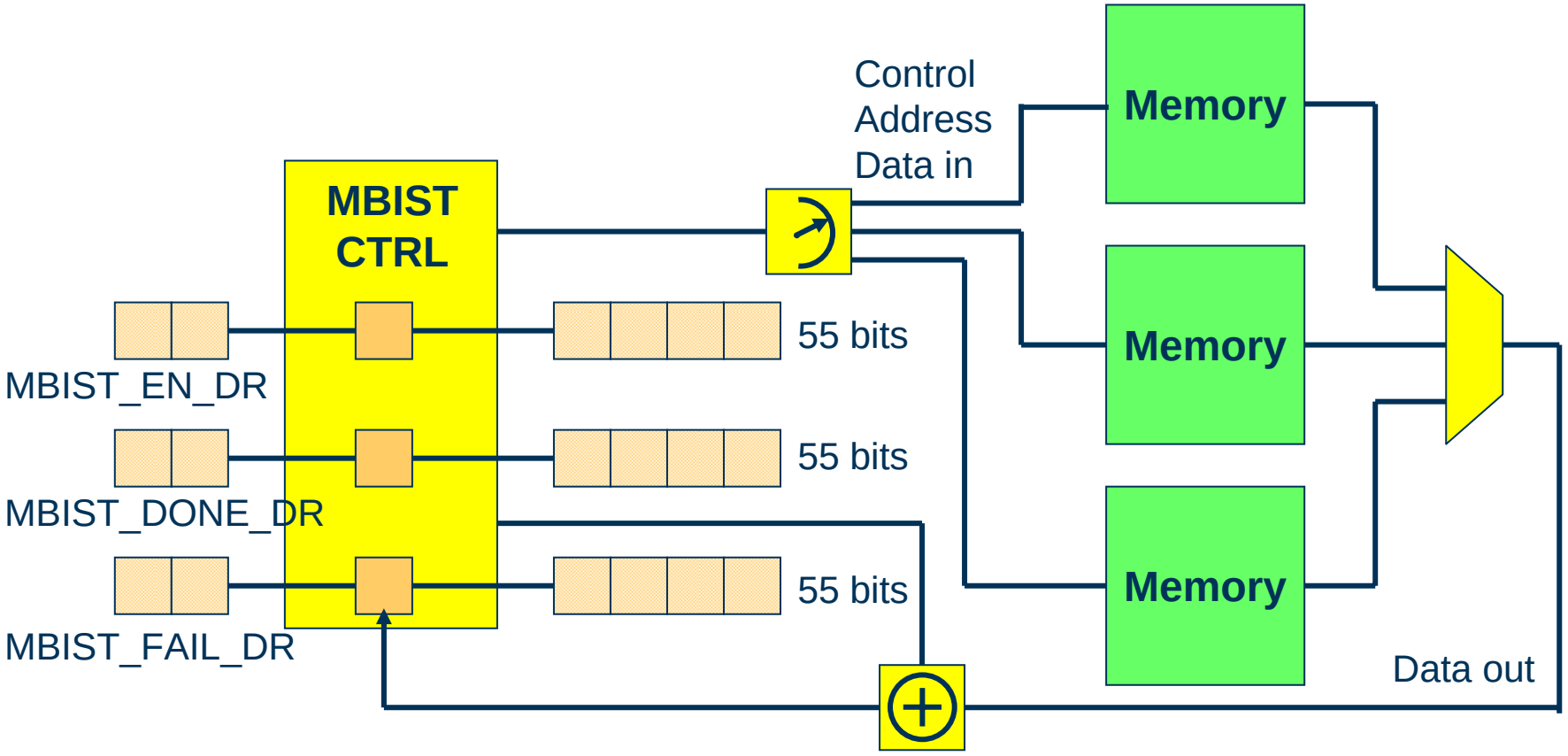


Conceptual DFT Architecture

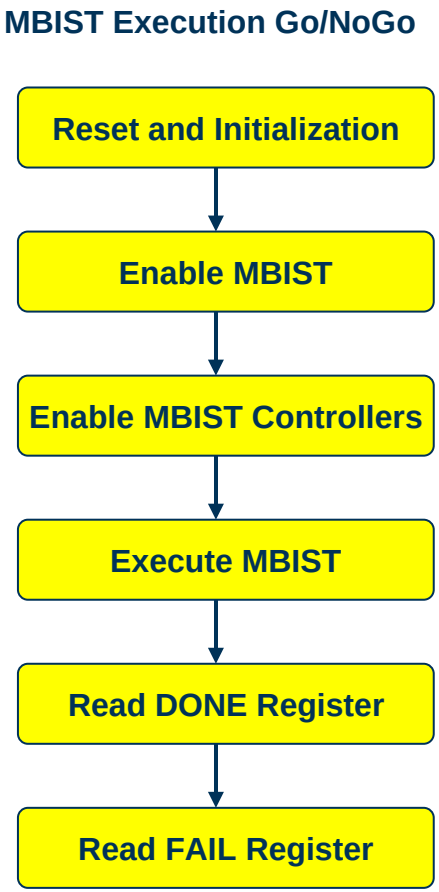
The real ASIC's have 55 MBIST controllers and 9 LBIST controllers each



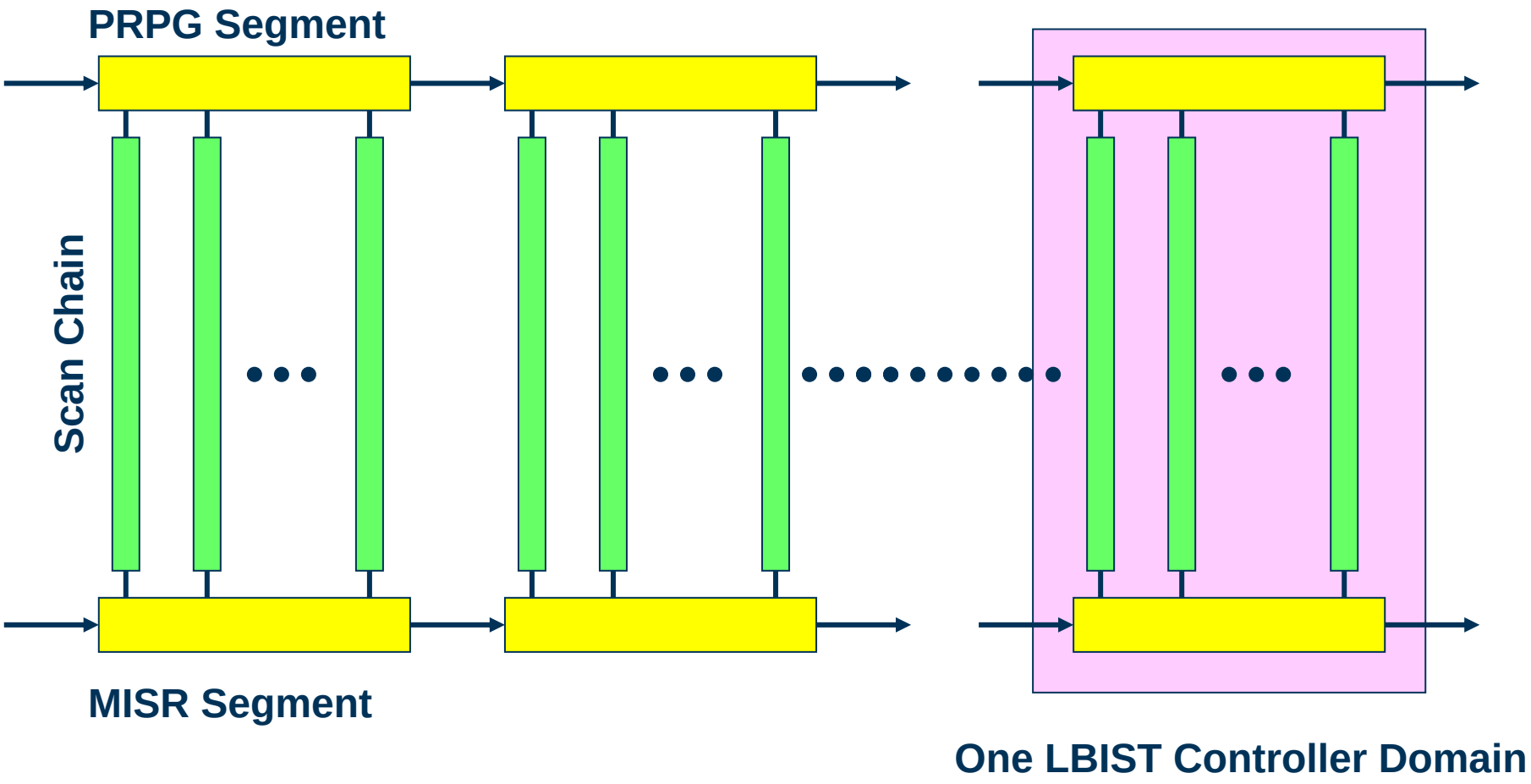
One MBIST Controller



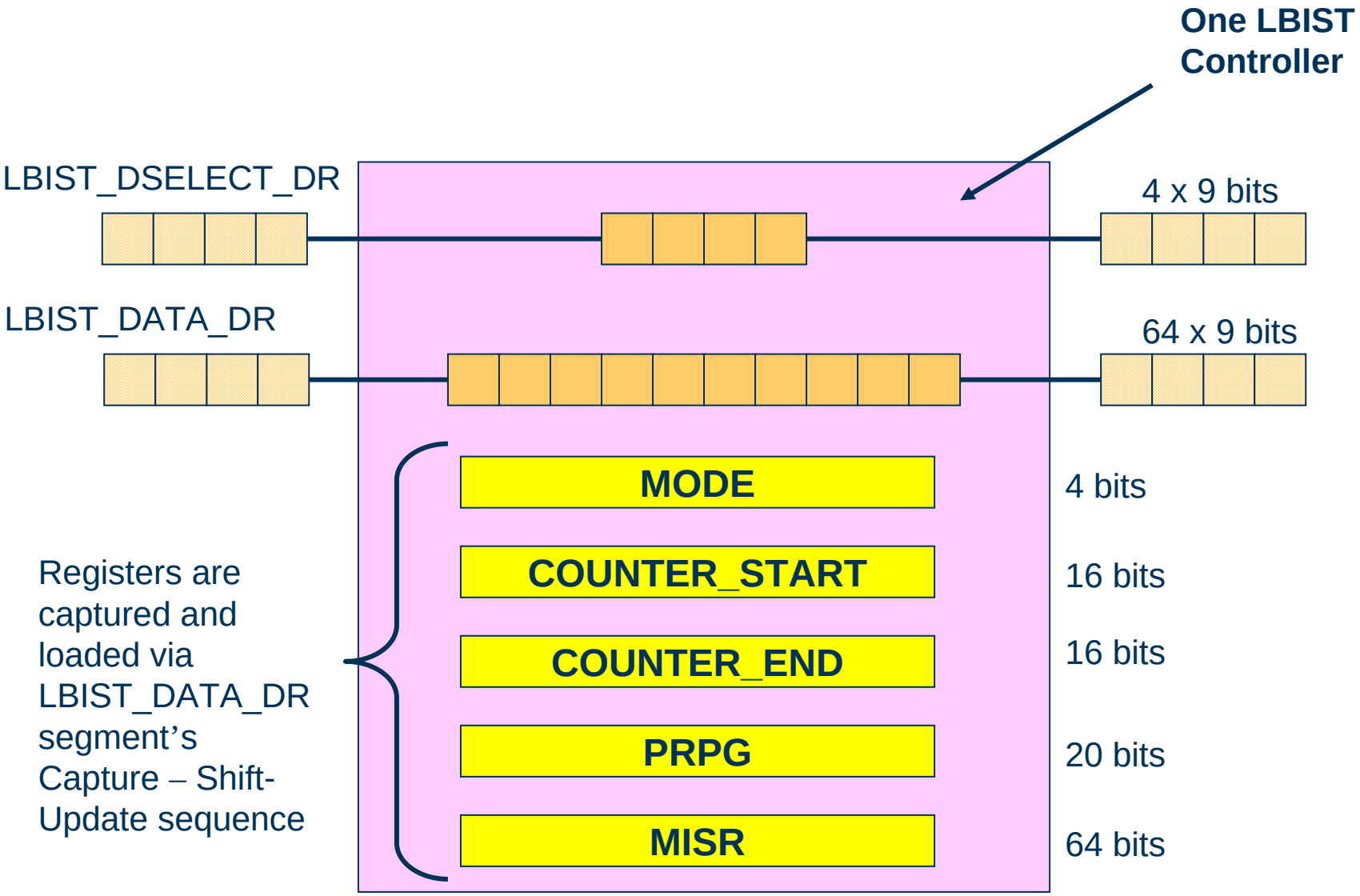
MBIST Execution Flow



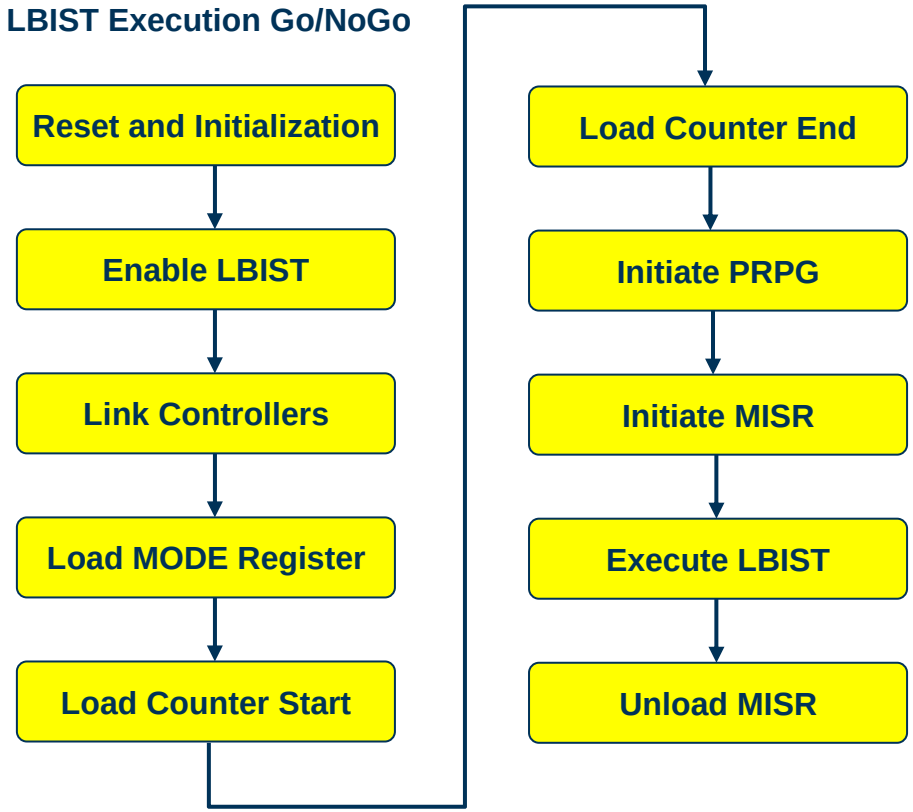
LBIST PRPG and MISR Configuration



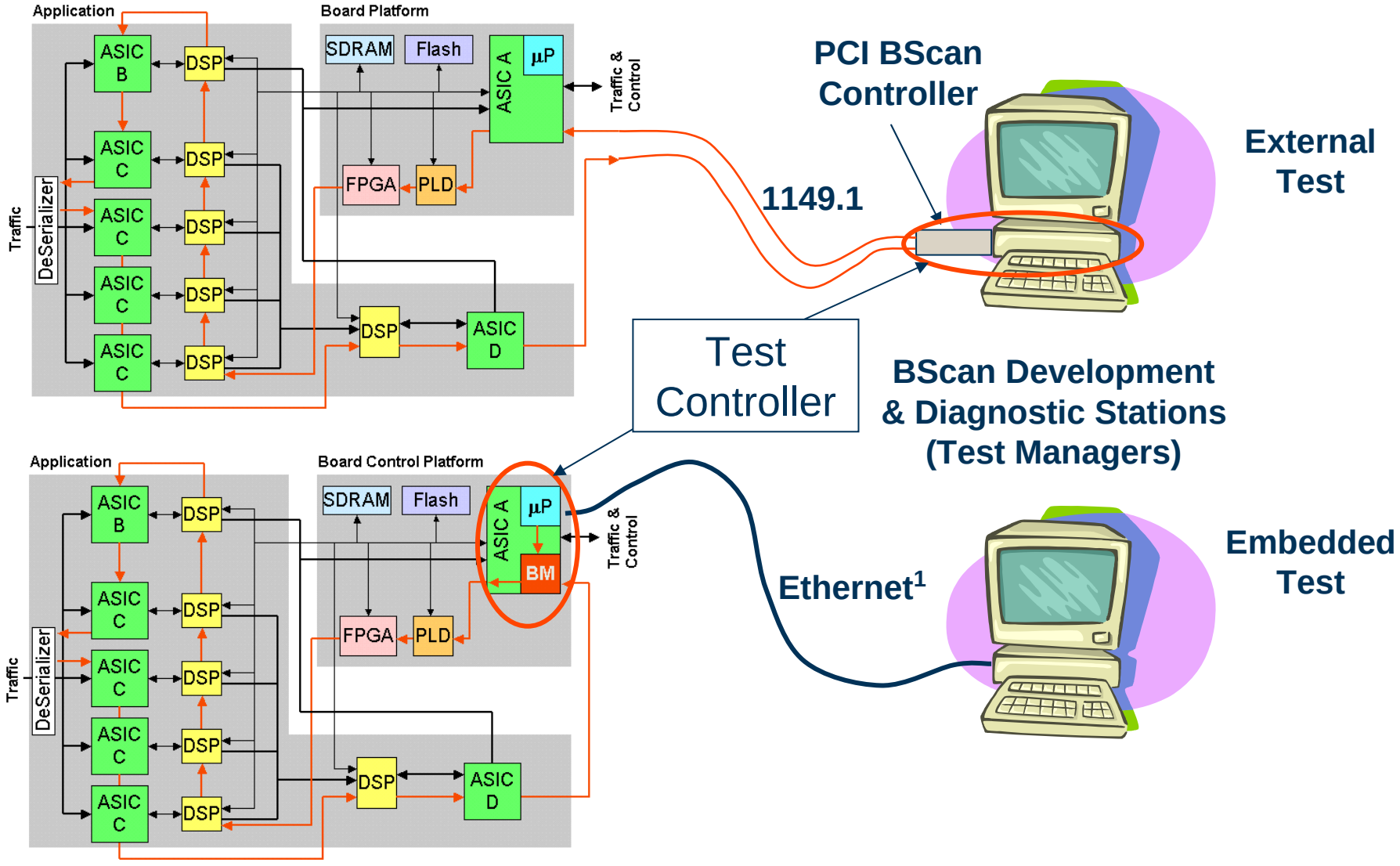
LBIST Controller Registers



LBIST Execution Flow



Debug and Diagnosis - HW View



1) Or other standard link

MSc Experiment

Legend

= Test Platform

= Board SW

= Modified TP SW

= New SW (Altera based)

PPC based SW
”Test Controller”

STAPL++ Player

MTC driver

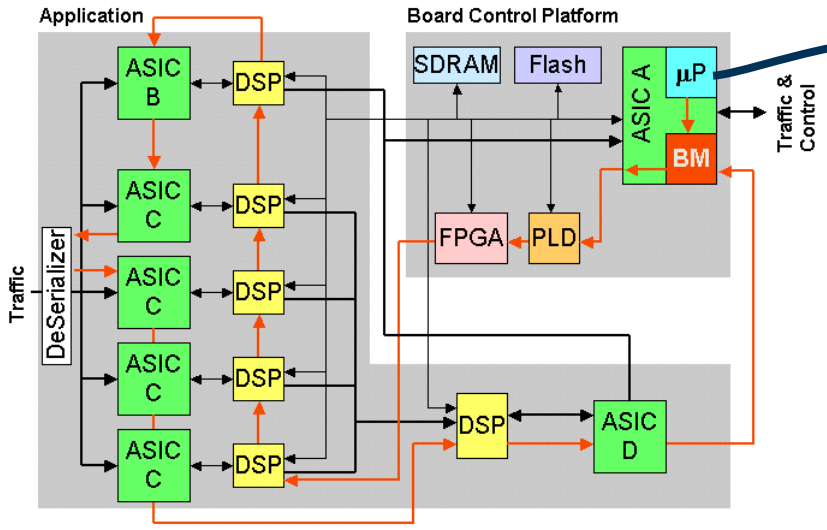
PC based SW
”Test Manager”

Idefix Test Shell

BScan Developm. & debug

Ericsson Test control SW

Commands:
Stop-on-fail
Run Action A
Run Procedure B
Return:
Failing vector
Execution trace



Ethernet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