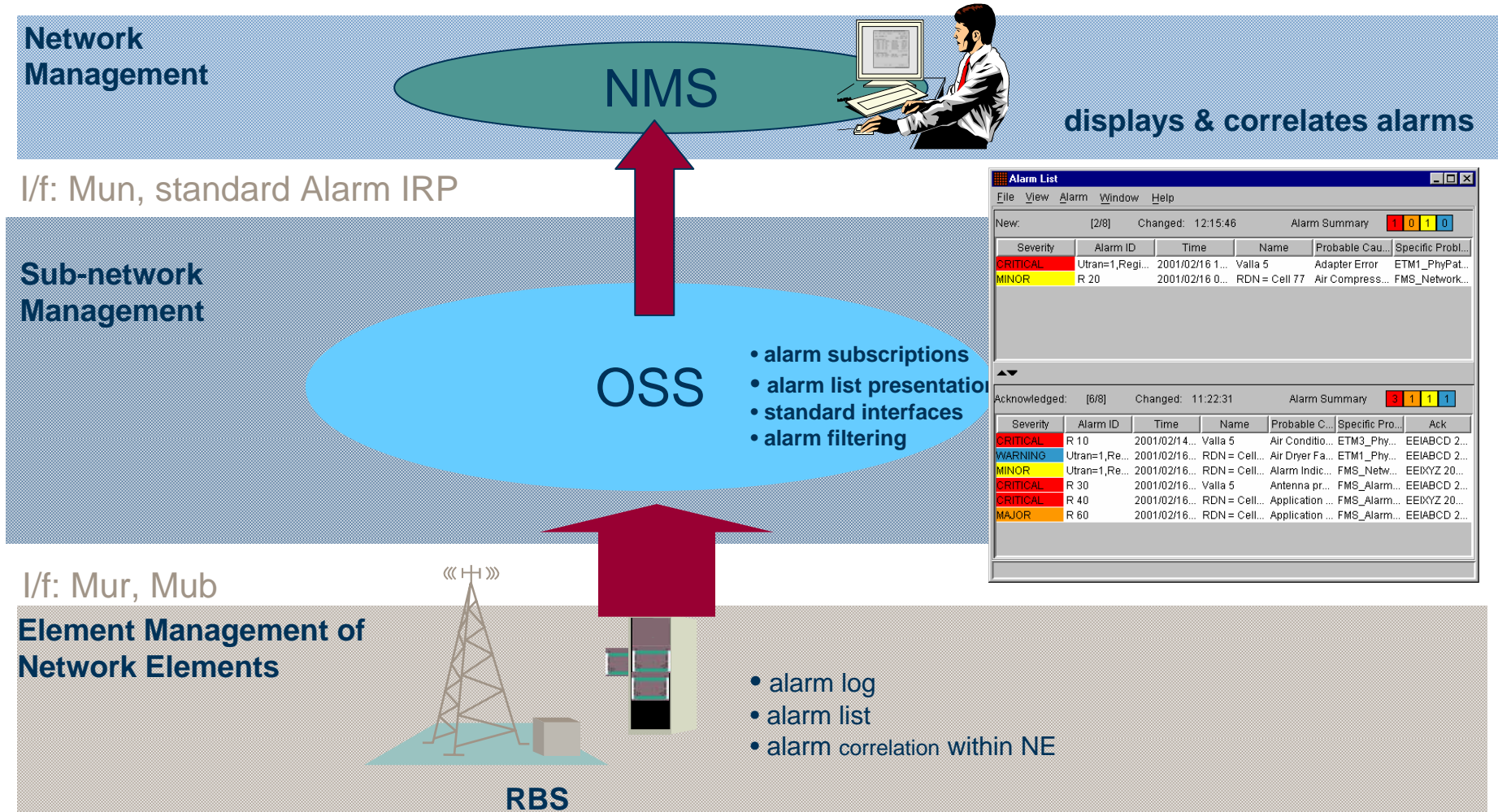


SJTAG in RBS at Ericsson

November 15, 2006

A Network Management View



Alarm Display

Alarm List

File View Alarm Window Help

New: [2/8] Changed: 12:15:46 Alarm Summary **1 0 1 0**

Severity	Alarm ID	Time	Name	Probable Cau...	Specific Probl...
CRITICAL	Utran=1,Regi...	2001/02/16 1...	Valla 5	Adapter Error	ETM1_PhyPat...
MINOR	R 20	2001/02/16 0...	RDN = Cell 77	Air Compress...	FMS_Network...

▲▼

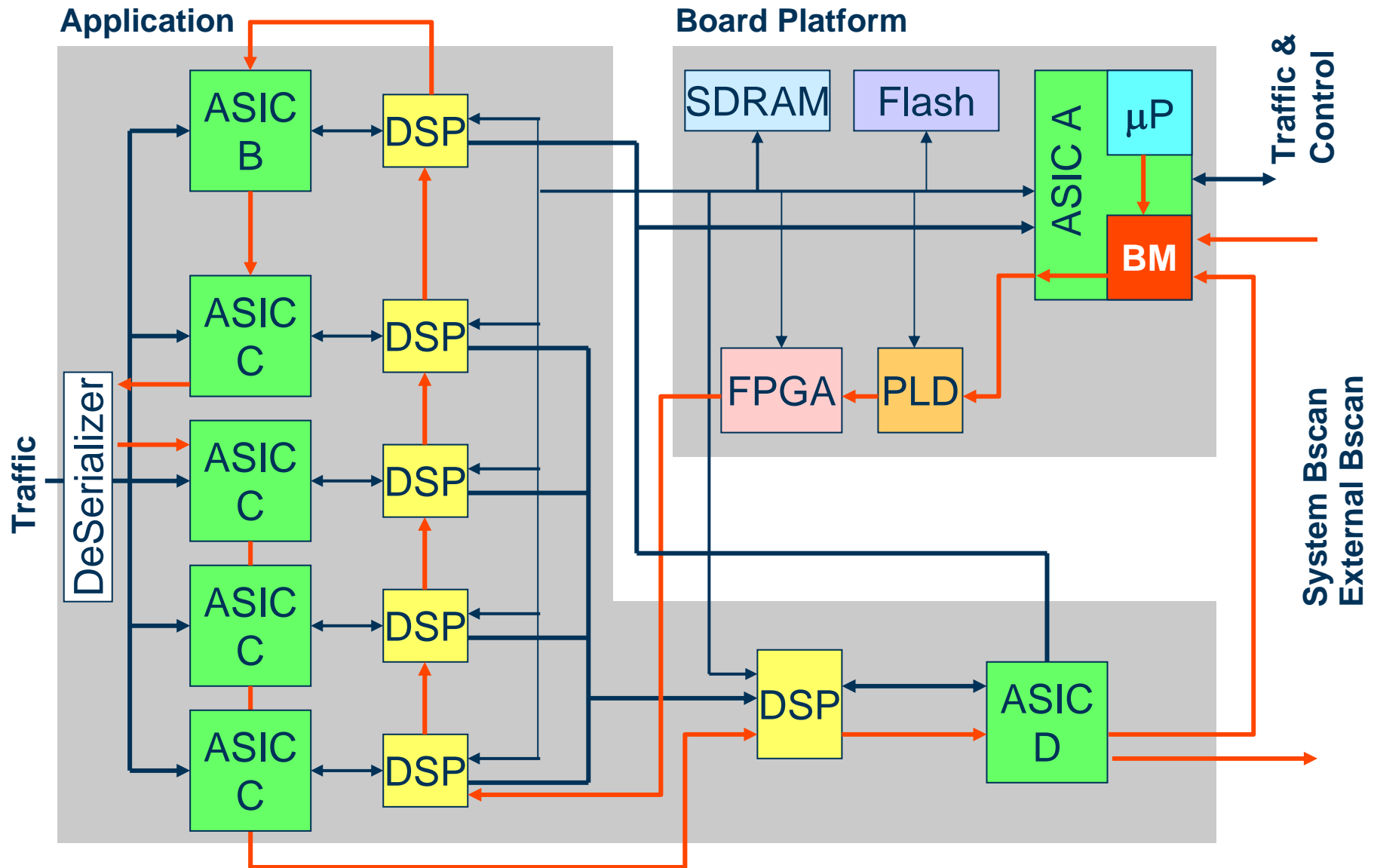
Acknowledged: [6/8] Changed: 11:22:31 Alarm Summary **3 1 1 1**

Severity	Alarm ID	Time	Name	Probable C...	Specific Pro...	Ack
CRITICAL	R 10	2001/02/14...	Valla 5	Air Conditio...	ETM3_Phy...	EEIABCD 2...
WARNING	Utran=1,Re...	2001/02/16...	RDN = Cell...	Air Dryer Fa...	ETM1_Phy...	EEIABCD 2...
MINOR	Utran=1,Re...	2001/02/16...	RDN = Cell...	Alarm Indic...	FMS_Netw...	EEIXYZ 20...
CRITICAL	R 30	2001/02/16...	Valla 5	Antenna pr...	FMS_Alarm...	EEIABCD 2...
CRITICAL	R 40	2001/02/16...	RDN = Cell...	Application ...	FMS_Alarm...	EEIXYZ 20...
MAJOR	R 60	2001/02/16...	RDN = Cell...	Application ...	FMS_Alarm...	EEIABCD 2...

EBST – Usage and Requirements

- Field test purposes
 - Validate HW fault related alarms, pinpoint replaceable unit
 - Detect latent faults at (re)start of boards or at regular tests
- Bscan test in the field
 - BScan is part of embedded test SW
 - Trade-off between test time and coverage
 - Diagnosis down to replaceable unit often sufficient
- In-system diagnostic test
 - Used at repair centers
 - Requires better coverage and diagnostic resolution
 - Not time critical

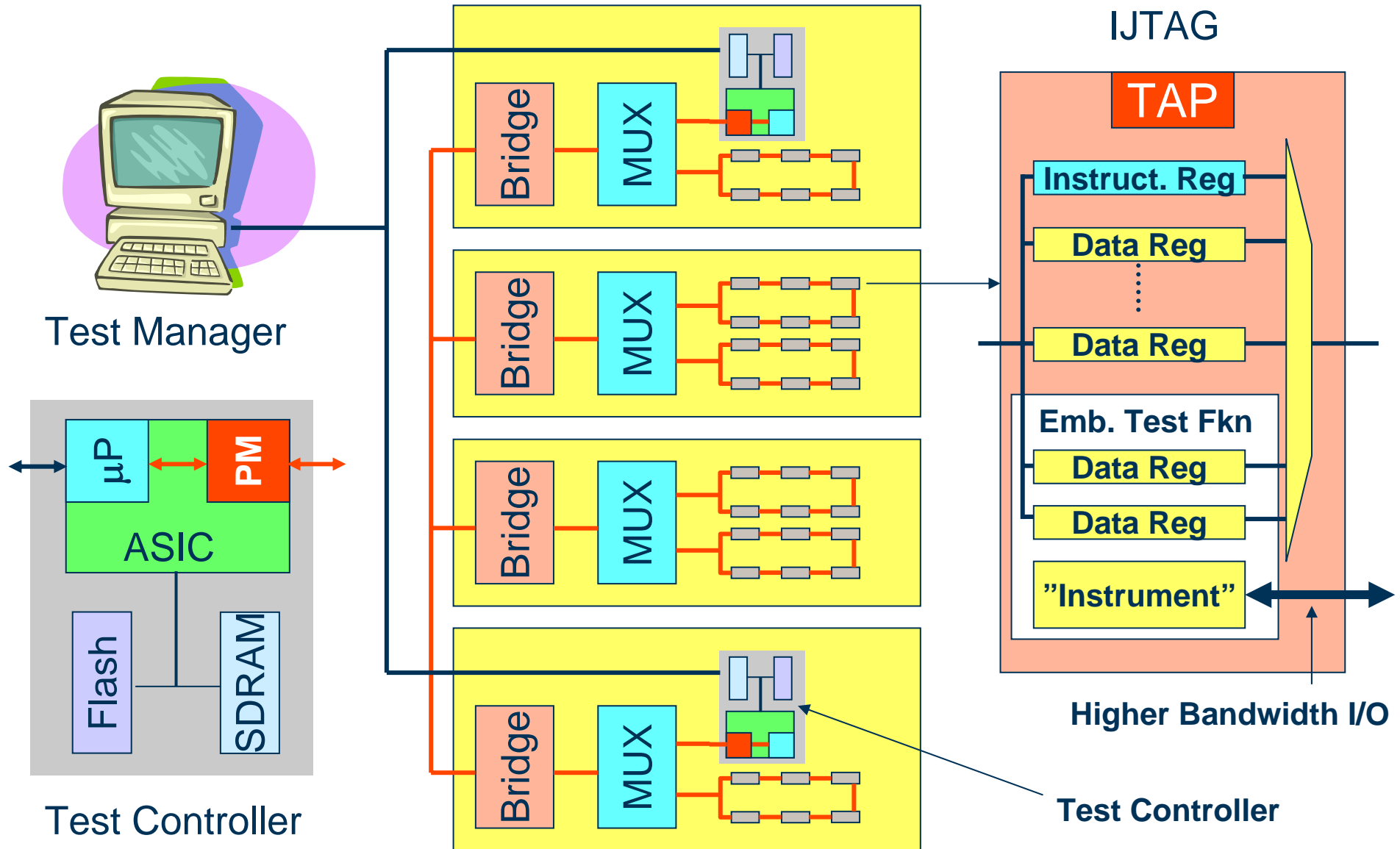
Embedded Boundary Scan Test



Typical EBST Operations

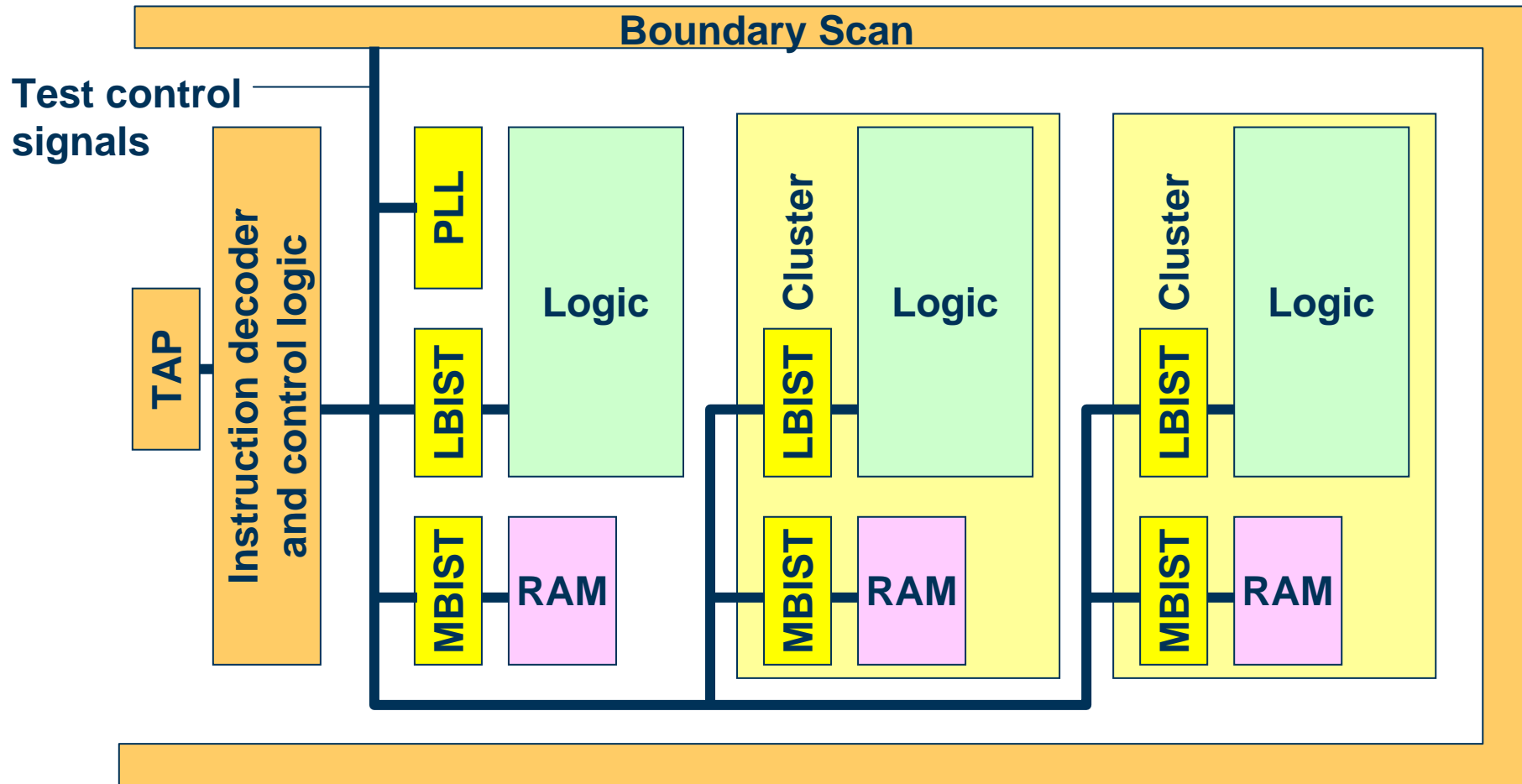
- Conventional (single board) interconnect test
 - Supported by SVF/STAPL standard languages
- In-system programming
 - Supported by STAPL
- System interconnect test using chain configuration devices (bridges, scan routers)
- Simple IJTAG operations (single board, no hierarchy)
- Complex IJTAG operations (through system and device hierarchies)

SJTAG and IJTAG

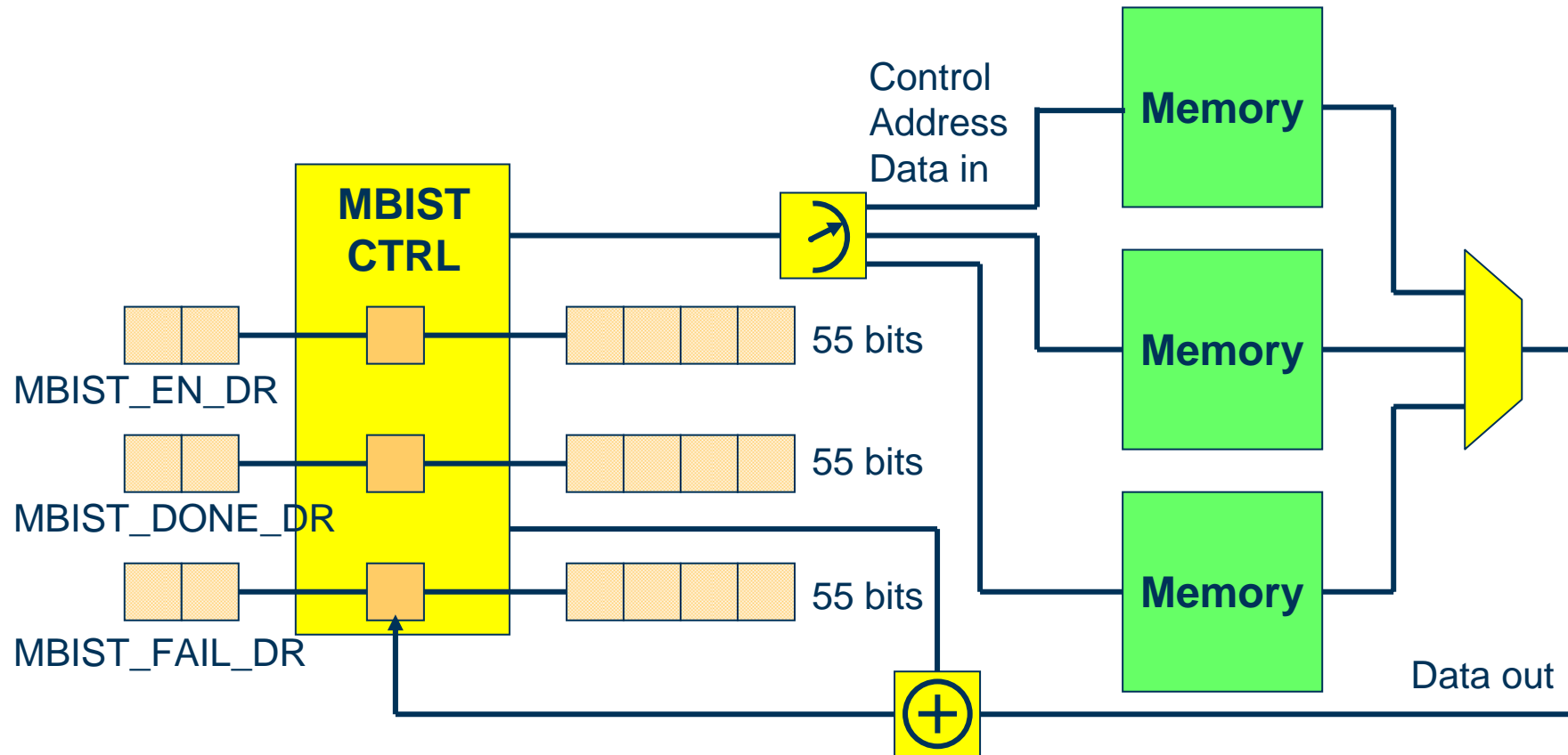


Conceptual DFT Architecture

The real ASIC's have 55 MBIST controllers and 9 LBIST controllers each

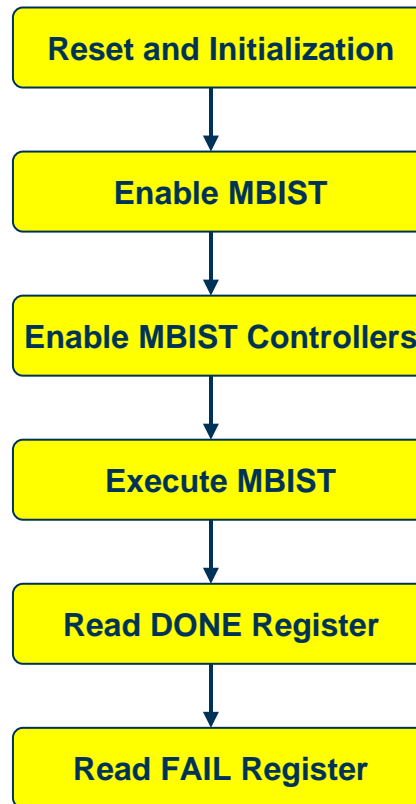


One MBIST Controller

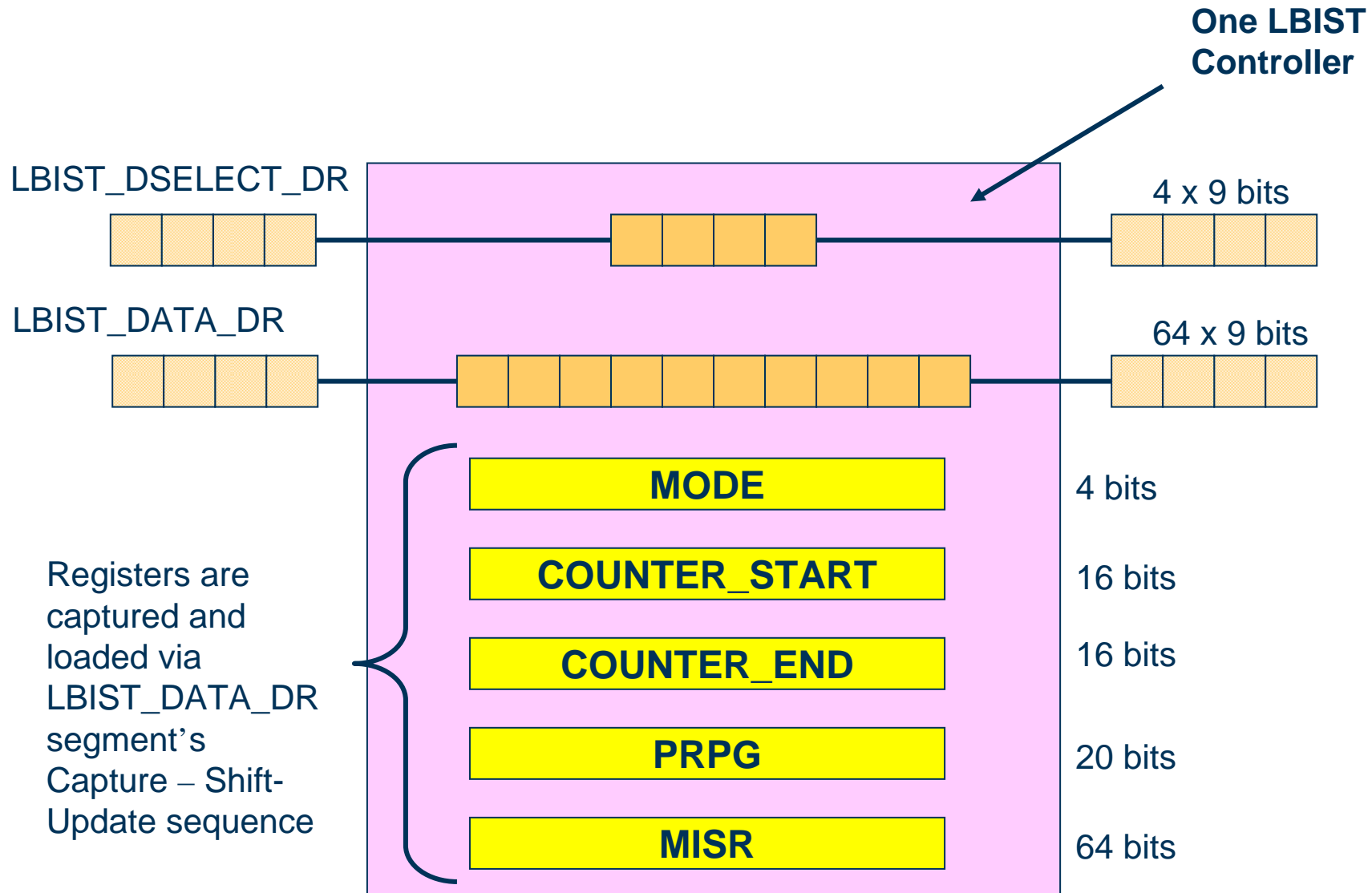


MBIST Execution Flow

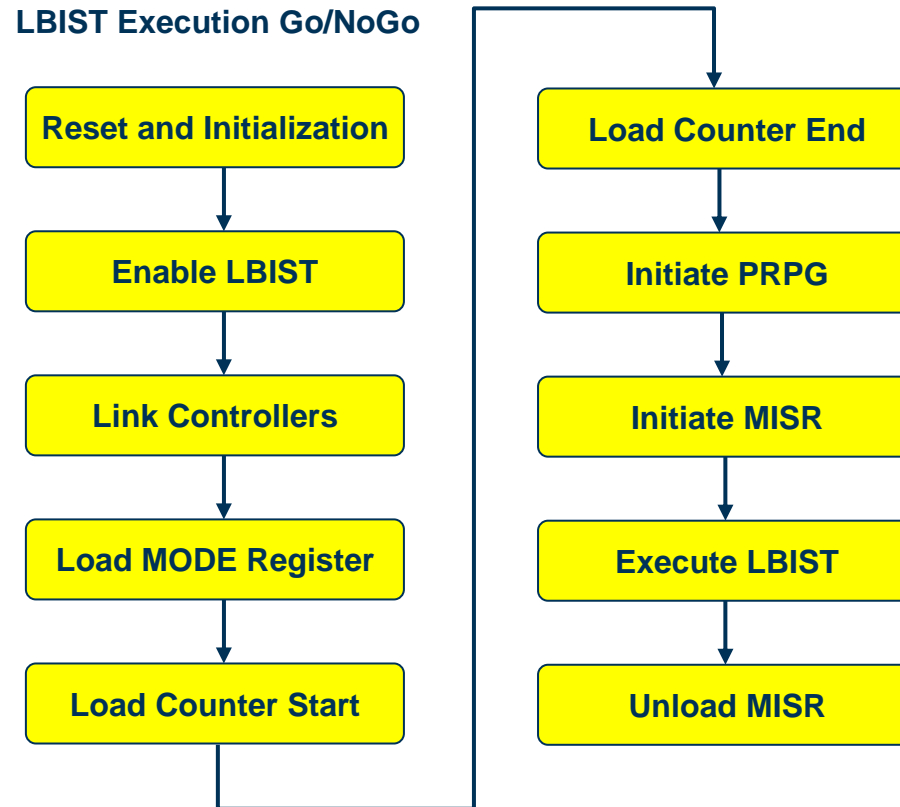
MBIST Execution Go/NoGo



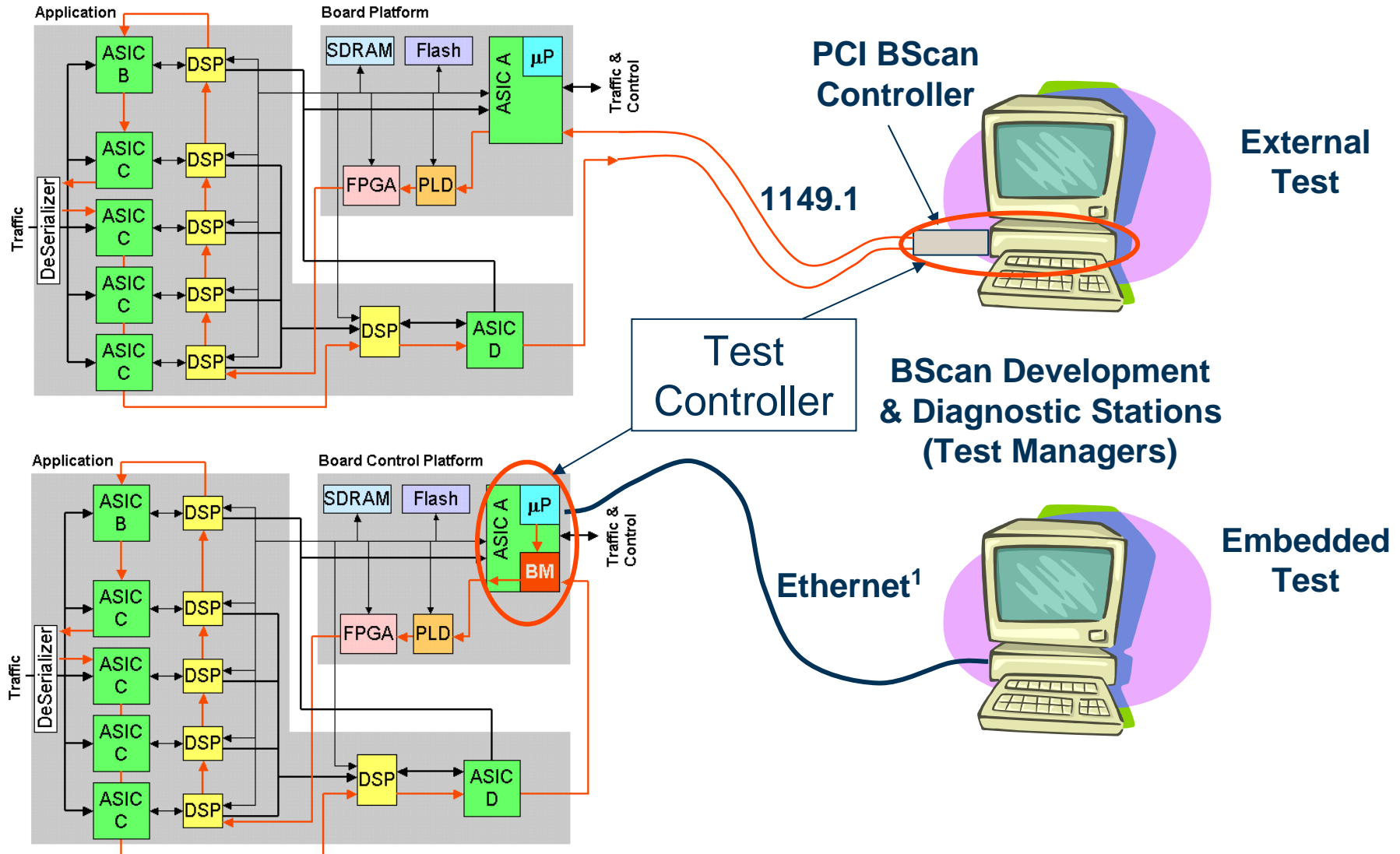
LBIST Controller Registers



LBIST Execution Flow






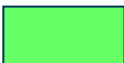
Debug and Diagnosis - HW View



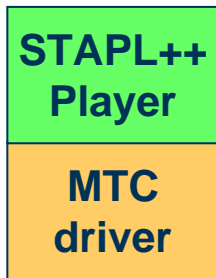
1) Or other standard link

MSc Experiment

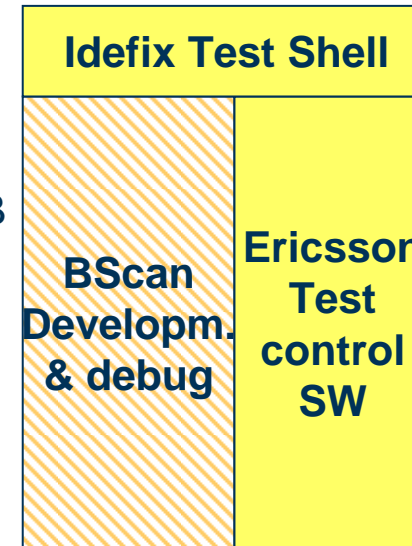
Legend

-  = Test Platform
-  = Board SW
-  = Modified TP SW
-  = New SW (Altera based)

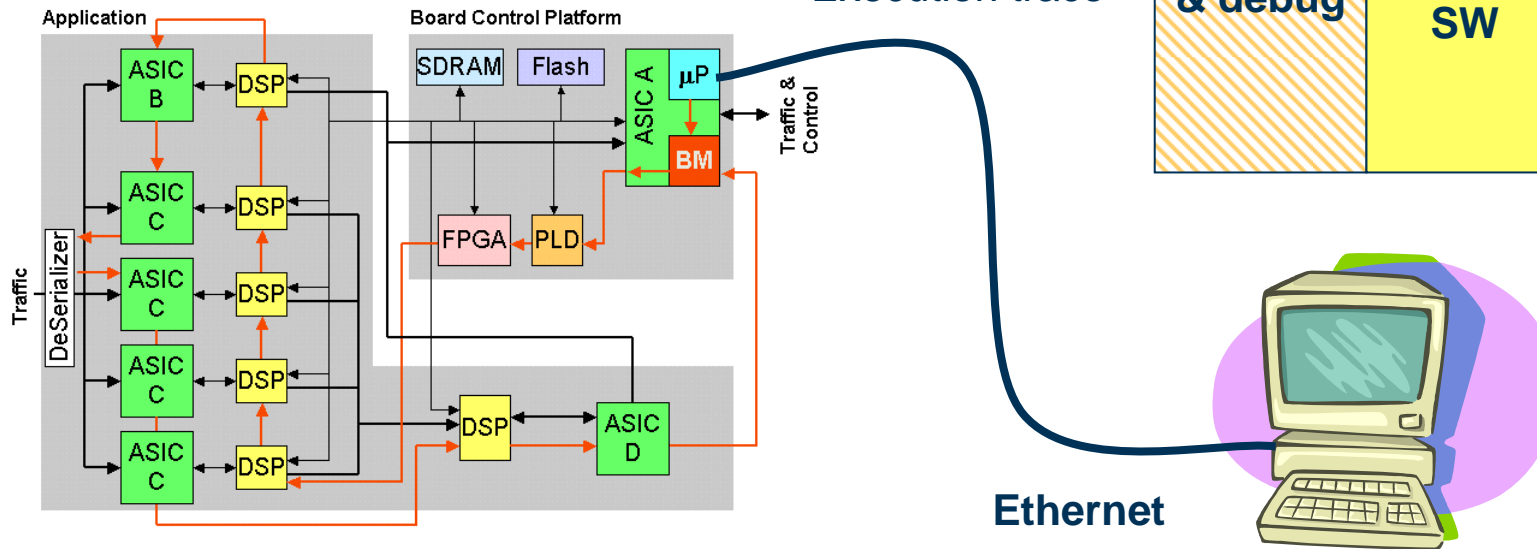
PPC based SW "Test Controller"



PC based SW "Test Manager"



Commands:
 Stop-on-fail
 Run Action A
 Run Procedure B
 Return:
 Failing vector
 Execution trace



ERICSSON 

TAKING YOU FORWARD