Status of SJTAG activity for ATCA Use Case

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ATCA Background

Background of JTAG in ATCA

- Original ATCA specification did not include JTAG
- Advanced Mezzanine Card (AMC) specification provided JTAG as an option to the board edge
- MicroTCA provided support for access to the AMC JTAG from the system level
- During the ATCA revision R3.0 change request cycle, JTAG integration was officially tracked under CR 4672

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Background of JTAG in ATCA

- Legacy ad hoc designs currently retarget the Metallic Test Bus and Ring Test Bus signals as Multi-drop JTAG interface to blades
- Ad hoc discussion group requesting the use of 4 reserved pins on Zone 1 connector to be designated for JTAG use in all slots

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Use Cases

Use Case Categorization

- Structural Test
- Configuration/Tuning/Instrumentation
- Software Debug
- Built-In Self Test (BIST)
- Fault Injection
- Programming/Updates
- Root Cause Analysis/Failure Mode Analysis
- Power-On Self Test (POST)
- Environmental Stress Test (EST)
- Device Versioning

Structural Test

- **Problem:** Verify connectivity between devices, mezzanines, and blades.
- **JTAG Test Solution:** Traditional IEEE Std. 1149.1interconnect test, cluster tests, memory tests
  - Scan Path Integrity
  - Board Interconnect
  - AMC Interconnect
  - AMC/Carrier Interconnect
  - Blade/Blade Interconnect
  - Device Cluster Interconnect
  - Memory Interconnect
  - Intel IBIST® PCIe Interconnect
- **Status:** ATPG from CAD for interconnect tests. ATPG from CAD and device models for cluster and memory. Manually generated tests for clusters.

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Structural Test

- **Required Technologies:**
  - Traditional ATPG requires devices to be 1149.1 compliant for full test coverage
  - Traditional ATPG may tolerate non-1149.1 devices on nets as long as these devices may be isolated from net yielding partial test coverage
  - Traditional ATPG requires devices to be 1149.6 compliant for pins wired to AC Coupled nets for full coverage (shorted capacitor will allow 1149.1 to pass)
  - Cluster requires full encapsulation of circuit with 1149.1 enabled devices along with regular structured logic to yield full test coverage
  - Test within a system requires constraints on externally accessible interface signals

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Configuration/Tuning/Instrumentation

- **Problem:** Dedicated registers in a device perform specific mission tasks. These registers must be accessed while the system is active to perform configuration, tuning, or special instrumentation features.
- **JTAG Test Solution:** Use embedded controller or external PC tester to access these registers using the system boundary-scan port to read/write new values from/to each register.
- **Status:** Feasibility has been demonstrated with current ad hoc techniques using proprietary interfaces over a system level multi-drop interface. IEEE Std. P1687 IJTAG will provide a common interface method to these registers providing the ability for more automation and interactive human interfaces.

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Configuration/Tuning/Instrumentation

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version to identify blade feature set
- **Optional Technologies:**
  - Chain isolation logic for target device and its respective registers

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Software Debug

- **Problem:** S/W hangs or is stuck in infinite loop
- **Test Solutions:** Query Boundary Scan Register (BSR) using SAMPLE mode to observe CPU pin states. Use boundary-scan to trigger NMI to initiate CPU dump operation. Ideally, use vendor emulation tools to capture state of CPU registers (PC, SP, Flags, Registers, etc.), but this requires more than 4 TAP wires.
- **Status:** SAMPLE mode already proven/used for Failure Signature Capture. Boundary-scan based Fault Injection already provides support for NMI trigger.

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Software Debug

- **Problem:** Blade software fails without indication of where the problem is located (e.g., unhandled alarm, unhandled overrun error)
- **JTAG Test Solution:** Once IEEE Std. P1149.7 becomes available and is supported in target processors, access to the internal registers of the processor is possible through a 4 wire TAP interface.
- **Status:** Current emulation interfaces require more signals than the 1149.1 4 wire TAP to control the emulation features of a processor. Some existing interfaces allow for some access of processor information using standard 1149.1 access. Most others use the TAP as a redefined interface.

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Software Debug

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version to identify blade feature set
  - A description of the chain topology to the processor
- **Optional Technologies:**
  - Chain isolation logic for target processor
  - Concurrent access to multiple processors

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Built-In Self Test (BIST)

- **Problem:** To test a device for its functionality and internal structure throughout its life cycle
- **JTAG Test Solution:** Use boundary scan at a board or system to enable device-level BIST
  - At device DFT
    - logic/memory BIST must be implemented in ASICs
    - BIST must be made accessible via boundary scan, e.g. RUNBIST
  - At board/system DFT, boundary scan test bus must be implemented
    - Access ASIC BIST
    - Download FPGA BIST configurations
- **Status:** Enabled via RUNBIST instruction or vendor PRIVATE instructions.

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Built-In Self Test (BIST)

- **Required Technologies:**
  - Boundary Scan Description Language (BSDL) file must define the RUNBIST instruction or vendor PRIVATE instructions used for test control
  - IEEE Std. P1687 Instrument JTAG (IJTAG) could be used in the future to enable concurrent BIST operations of multiple cores within a device
  - FPGA BIST requires new firmware images which may be reused from foundry testing with optional USER registers providing JTAG access to BIST logic

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Fault Injection

- **Problem:** During system integration test, hardware fault injection facilitates the development and verification of the diagnostic software of highly reliable systems
- **Test Solution:** Using existing boundary scan architecture of FPGAs and ASICs to achieve “virtual” pin-level fault injection
  - replace expensive physical fault injection
  - higher fault injection coverage
- **Status:** Papers presented on this subject at ITC for FPGA and ASIC versions of boundary-scan based fault injection demonstrating capability.

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Fault Injection

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version
  - A description of the chain topology
  - A description of the internal registers for faulting devices in the BSDL file

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Firmware Programming/Updates

- **Problem:** Program/update of programmable devices such as cPLDs, FPGAs etc. during prototype and volume production as well as in the field
- **JTAG Test Solution:** Use embedded controller or external PC tester to apply programming sequence via system boundary-scan port.
- **Status:** Commonly used for field updates and prototype model updates for blades not resident in hardware design lab. Useful as remote access update tool using common process for all FPGA/CPLD updates.

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Firmware Programming/Updates

- **Problem:** Program/update of programmable devices such as FLASH Memory during prototype and volume production as well as in the field
- **JTAG Test Solution:** Use embedded controller or external PC tester to apply programming sequence via system boundary-scan port to control FLASH interface signals as a logic cluster.
- **Status:** Commonly used for field updates when other means for updates are unavailable. Slow access to FLASH due to serial transmission nature of 1149.1. Unable to leverage hardware write pulse signal with just 4 TAP wires.

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Firmware Programming/Updates

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version
  - Access to repository of firmware update vector sequences

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Root Cause Analysis/Failure Mode Analysis

- **Problem:** Blade software fails without indication of where the problem is located or blade locks up and becomes unresponsive
- **JTAG Test Solution:** IEEE Std. 1149.1 provides a non-intrusive SAMPLE mode to sample the value of the device pins while the device is in non-test mode. Thus, alarm signals or other state information may be extracted from a blade using the System Boundary-Scan interface
- **Status:** SAMPLE access to device pins has been used for both the Boundary-Scan Register (BSR) at the device pins as well as registers within a device's design. Ideal for monitoring inaccessible signals.

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Root Cause Analysis/Failure Mode Analysis

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version
  - A description of the chain topology
  - A description of the internal registers in the BSDL file

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Power-On Self Test

- **Problem:** Verify Interconnections during initial power-on of a system
- **JTAG Test Solution:** Perform a system boundary-scan test of each blade during boot. Time constraints need to be considered. Useful for unresponsive blades.
- **Status:** System level access to blades occurs one at a time when 4 wire JTAG is used. Thus, total test time is additive and unable to be concurrent. Suggest implementing local boundary-scan test on a blade for concurrent POST.

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Power-On Self Test (POST)

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version in test vectors are not stored on the blade
  - Access to correct set of tests for the blade under test
  - Optional access to test vector information stored on the UUT

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Test Stimulus During EST (Environmental Stress Test)

- **Problem:** Detect and rapidly locate intermittent solder connections. Without test stimulus application, the test effectiveness is greatly impaired. These are generally required test activities for telecommunication corporate customers.
- **Test Solution:** Apply boundary-scan while blade/system is under stress (EST)
- **Status:** Externally driven and embedded applications to *leverage board level and system level boundary-scan capability designed into product*.

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Test Stimulus During EST (Environmental Stress Test)

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version
  - A description of the chain topology
  - A description of the internal registers in the BSDL file

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Device Version Identification

- **Problem:** Recognizing/Verifying the device types and versions installed on a board
- **Test Solution:** Query Boundary-Scan *IDCODE* register
- **Status:** Verification already performed by required Scan Path Integrity test. Specialized queries may be easily developed targeting specific devices.
- *This feature may be used during installation and field support to identify/confirm device version relating to S/W and H/W field failures.*

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Device Version Identification

- **Required Technologies:**
  - Access to each blade's JTAG from the mid-plane
  - Information regarding the blade type and version
  - A description of the chain topology
  - A description of the IDCODE register for target devices in the BSDL file

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Goals

Dream goals for successful JTAG in ATCA

Interoperability

- Provide an interface that maximizes JTAG interoperability across all vendor blades
- Provide an interface that is protocol neutral in management of the connections to each blade while compatible with IEEE Std. 1149.1
- Provide an interface that supports current and future IEEE Std. 1149.1 enabled operations at the device, board, and system scope (e.g. IEEE Stds. 1149.6, 1532, P1149.7, P1687, P1581, IBIST®, …)

Dream goals for successful JTAG in ATCA
Interoperability

- Multiple vendor interoperability for JTAG test through Carrier Blades
- ATCA Carrier Blade architectures must provide for multi-vendor JTAG interoperability at backplane and mezzanine scopes

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Dream goals for successful JTAG in ATCA
Access

- Provides access to JTAG infrastructure from external test equipment without removing panels or blades
- Provides access to JTAG infrastructure from embedded test resources
- Provisions redundant support of JTAG operation
- Does not require JTAG support on blades that do not contain JTAG equipped devices

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Dream goals for successful JTAG in ATCA
Access

- Support for access to hierarchical JTAG architectures on blades (especially ATCA Carrier Blades)
- Co-existing interface from backplane with local JTAG infrastructure

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Dream goals for successful JTAG in ATCA
Operation

- Provide an interface that allows for changes in signal properties (e.g., signal levels) without changes to the test tooling and architecture
- System level JTAG chain topology must be immune to changes in the system blade configuration
- ATCA Carrier Blade architectures must be immune to changes in the AMC blade configuration

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Dream goals for successful JTAG in ATCA
Operation

- Supports “hot swap” of blades within the system
- Supports testing of blades with minimal blade resources operational (e.g., Board Management Controller operational with power to blade established) [Need to identify use cases showing minimal resources necessary for diagnostics]
- TRST needs to be managed by the blade locally without preventing test access from the backplane

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Dream goals for successful JTAG in ATCA
Performance

- Provides support for sustained 1149.1 operation at TCK frequencies up to 40MHz but must support the maximum frequency dictated by the blade design (e.g., lowest max frequency given in the slowest device BSDL)
- Provides JTAG signal integrity for all configurations of blade population

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Goals and Use Cases

Interoperability Goals

		Use Case Senarios									
	Goals	Structural Test	Configuration/ Tuning/ Instrumentation	Software Debug	BIST	Fault Injection	Programming/ Updates	Root Cause Analysis/ FMA	POST	EST	Device Versioning
Interoperability	Provide an interface that maximizes JTAG interoperability across all vendor blades	✓	✓	✓	✓	✓	✓	✓		✓	✓
	Provide an interface that is protocol neutral in management of the connections to each blade while compatible with IEEE Std. 1149.1										
	Provide an interface that supports current and future IEEE Std. 1149.1 enabled operations at the device, board, and system scope (e.g. IEEE Stds. 1149.6, 1532, P1149.7, P1687, P1581, IBIST®, ...)		✓	✓		✓					
	Multiple vendor interoperability for JTAG test through Carrier Blades	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	ATCA Carrier Blade architectures must provide for multi-vendor JTAG interoperability at backplane and mezzanine scopes	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Access Goals

	Goals	Structural Test	Configuration/ Tuning/ Instrumentation	Software Debug	BIST	Fault Injection	Programming/ Updates	Cause Analysis/ FMA	POST	EST
		Use Case Senarios								
Access	Provides access to JTAG infrastructure from external test equipment without removing panels or blades	✓	✓	✓	✓	✓	✓	✓		✓
Access	Provides access to JTAG infrastructure from embedded test resources	✓	✓		✓	✓	✓	✓	✓	✓
Access	Provisions redundant support of JTAG operation							✓		
Access	Does not require JTAG support on blades that do not contain JTAG equipped devices									
Access	Support for access to hierarchical JTAG architectures on blades (especially ATCA Carrier Blades)	✓	✓	✓	✓	✓	✓	✓	✓	✓
Access	Co-existing interface from backplane with local JTAG infrastructure	✓			✓			✓	✓	

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Operation Goals

	Goals	Structural Test	Configuration/ Tuning/ Instrumentation	Software Debug	BIST	Fault Injection	Programming/ Updates	Root Cause Analysis/ FMA	POST	EST
		Use Case Senarios								
Operation	Provide an interface that allows for changes in signal properties (e.g., signal levels) without changes to the test tooling and architecture	✓	✓	✓	✓	✓	✓	✓	✓	✓
Operation	System level JTAG chain topology must be immune to changes in the system blade configuration	✓								✓
Operation	ATCA Carrier Blade architectures must be immune to changes in the AMC blade configuration	✓								✓
Operation	Supports "hot swap" of blades within the system									
Operation	Supports testing of blades with minimal blade resources operational (e.g., Board Management Controller operational with power to blade established)	✓					✓	✓	✓	✓
Operation	TRST needs to be managed by the blade locally without preventing test access from the backplane			✓					✓	

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Performance Goals

		Use Case Senarios								
	Goals	Structural Test	Configuration/ Tuning/ Instrumentation	Software Debug	BIST	Fault Injection	Programming/ Updates	Root Cause Analysis/ FMA	POST	EST
Performance	Provides support for sustained 1149.1 operation at TCK frequencies up to 40MHz		✓				✓			
	Provides JTAG signal integrity for all configurations of blade population	✓	✓	✓	✓	✓	✓	✓	✓	✓

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