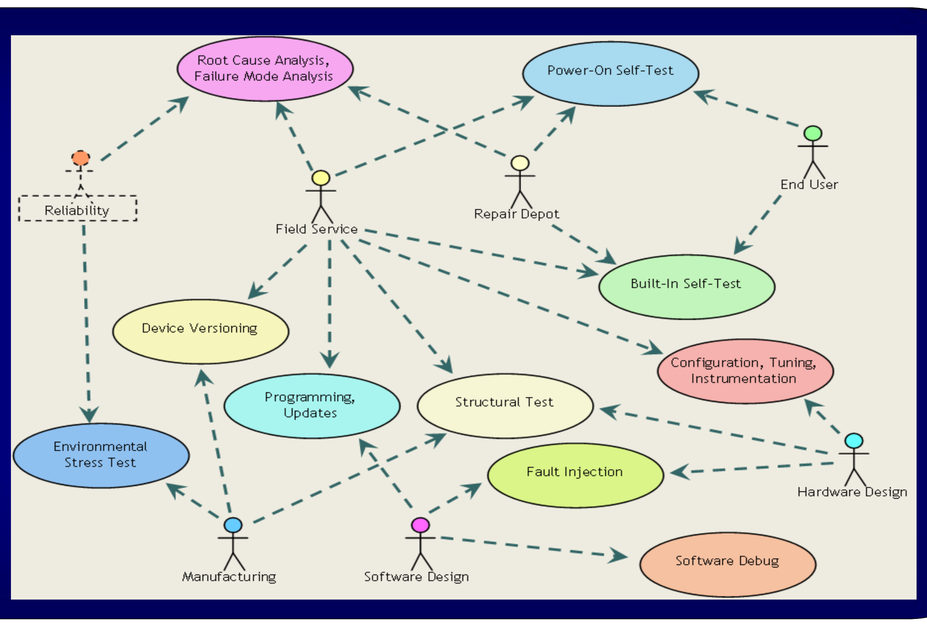
System Test Access Management

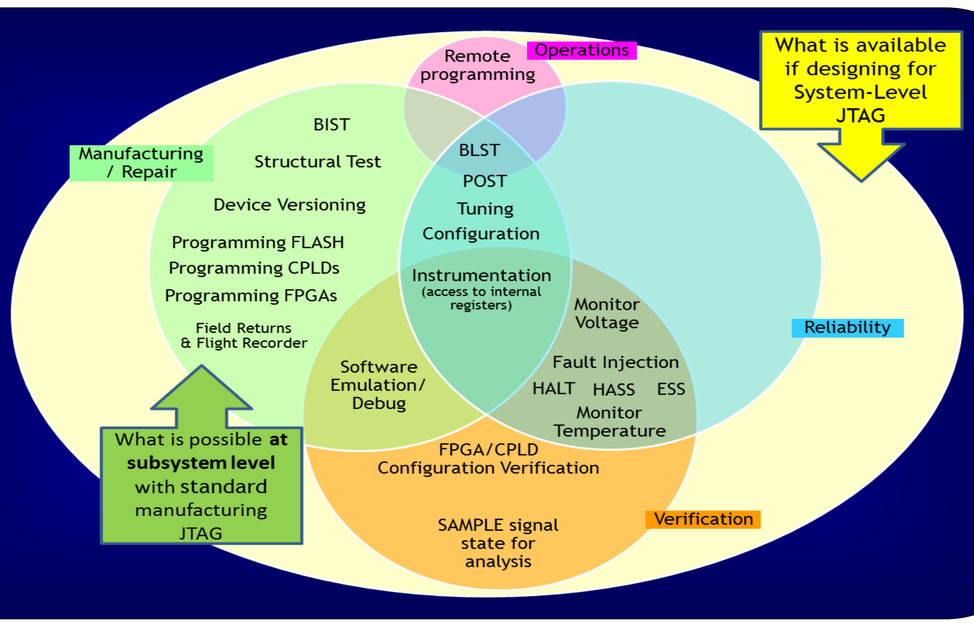
SJTAG Use Cases



System Definition

For the purposes of "System Test Access Management", a system may be described as an organized collection of components or assemblies that are designed to operate together to perform one or more tasks or functions.

SJTAG Universe



System Configurations

- ❖ TBD.

Concerns to Address

- ❖ Access to target (system topology)
- ❖ Data collection
- ❖ Data Analysis
- ❖ Diagnostics support
- ❖ Hand-off to other standards
- ❖ Test re-use through system hierarchy
- ❖ Black-box vs White-box test

SJTAG Timeline:

2005
- Creation of the System-level JTAG Initiative (SJTAG)

2006
- Survey of SJTAG Members

2009
- Survey of user and industry experts

2017
- Creation of System Test Access Management study group

2018?
- Submission of PAR
- Form IEEE TTSC sponsored Standard

202x?
- Initial version of a Standard for System Test Access Management

Regular meetings to identify problems, needs, requirements, analyze existing standards, etc.

Develop one or more Standards documents

http://www.sjtag.org/

Draft Need

- Existing standards focus on component level only
- **Coordination** at board and system level is needed for effective leverage of existing and future component level standards
- A supervisory standard is required to define **Coordination** and dependencies of instruments, and the configuration, management, and application of tests at the board and system levels

Draft Purpose

- Seamless integration of component access topologies, interface constraints, and other dependencies at the board and system level
- Uniform **description** of **topology** and **behavior**
- **Coordination** of access topologies through a set of familiar, interchangeable interfaces
- Routing data sets to particular destination registers in the correct time order

Draft Scope

- Leverage existing test interface standards by defining a description to better manage how they are used in the system
- **Coordination** and control of device, board, and sub-system test interfaces to extend access to the system level

Participating Organisations:

ARM❖ASSET Intertech❖ATE Solutions❖Cadence Design Systems❖Cisco Systems❖Curtiss-Wright Controls❖Dell❖DFT Solutions❖Firecron Ltd.❖GOEPEL Electronics❖Intel Corporation❖JTAG Technologies❖Keysight❖Leonardo MW Ltd.❖Marvell Inc.❖National Instruments❖NAVAIR Lakehurst❖Nokia❖Nvidia❖Schweitzer Engineering Laboratories, Inc.❖Via CPU Platform Inc.