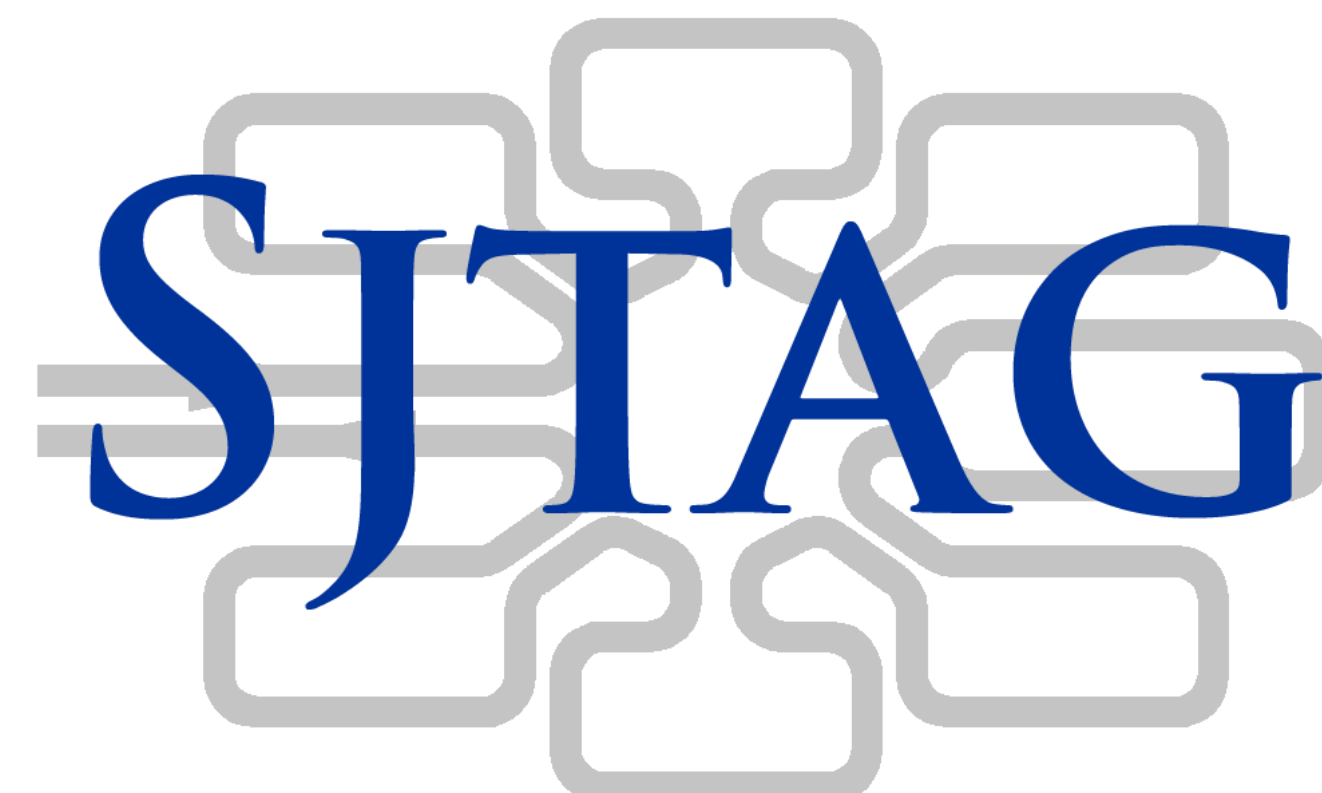
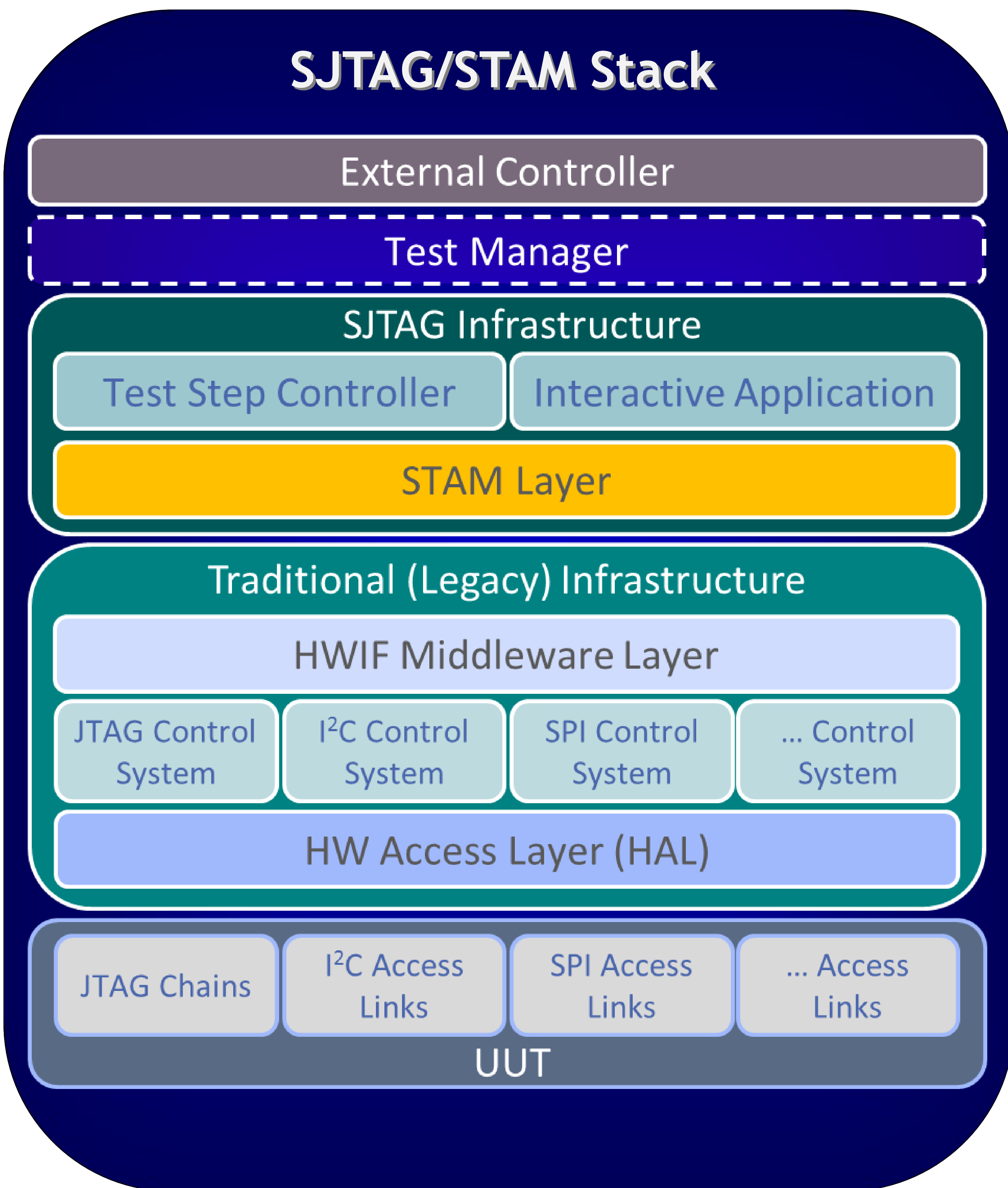


System Test Access Management (C/TT/STAM)



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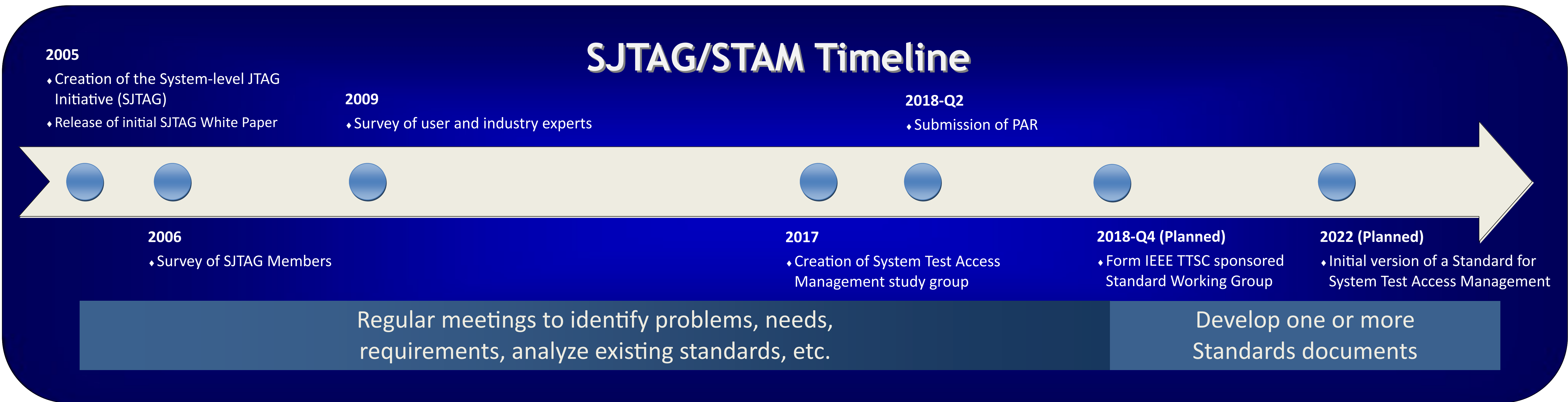


For the purposes of “System Test Access Management”, a system may be described as an organized collection of components or assemblies that are designed to operate together to perform one or more tasks or functions.

What is a System?

- ### Target Scenarios
- ❖ System on Chip
 - ❖ Multi Chip Module
 - ❖ Embedded computer
 - ❖ Automatic Teller Machine
 - ❖ Telecom base station
 - ❖ Automobile
 - ❖ Home security system
 - ❖ Airplane autopilot
 - ❖ Data center
 - ❖ ...

- ### Concerns to Address
- ❖ Access to target (system topology)
 - ❖ Data collection
 - ❖ Data Analysis
 - ❖ Diagnostics support
 - ❖ Hand-off to other standards
 - ❖ Test re-use through system hierarchy
 - ❖ Black-box vs White-box test



- ### Need
- ♦ Existing standards focus on component level only
 - ♦ **Coordination** at board and system level is needed for effective leverage of existing and future component level standards and to manage instrument dependencies

- ### Purpose
- ♦ Seamless integration of component access topologies, interface constraints, and other dependencies at the board and system level
 - ♦ Uniform **description** of **topology**, **interfaces** and **behavior**
 - ♦ **Coordinated** routing of data sets to particular destination registers in the correct time order

- ### Scope
- ♦ Use/re-use of test assets (e.g. device interfaces) to extend test access to board and system levels.
 - ♦ Does **not** define a new test interface but defines representations and methods to better use and **coordinate** those that are already present.

Participating Organisations:

ARM ❖ ASSET Intertech ❖ ATE Solutions ❖ Cadence Design Systems ❖ Cisco Systems ❖ Curtiss-Wright Controls ❖ Dell ❖ DFT Solutions ❖ Firecron Ltd. ❖ GOPEL Electronics ❖ Intel Corporation ❖ JTAG Technologies ❖ Keysight ❖ Leonardo MW Ltd. ❖ Marvell Inc. ❖ National Instruments ❖ NAVAIR Lakehurst ❖ Nokia ❖ Nvidia ❖ Schweitzer Engineering Laboratories, Inc. ❖ Via CPU Platform Inc.