



# How IEEE P1687.1 and IEEE P2654 can cooperate to access on-chip instruments during system assembly test

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# Outline

- Acronyms
- Board test use model
- Hierarchy, transitions and retargeting
- STAM bridge model
- Conclusions

## STAM

- System Test Access Management
- [IEEE P2654](#)

## SJTAG

- [System JTAG](#)

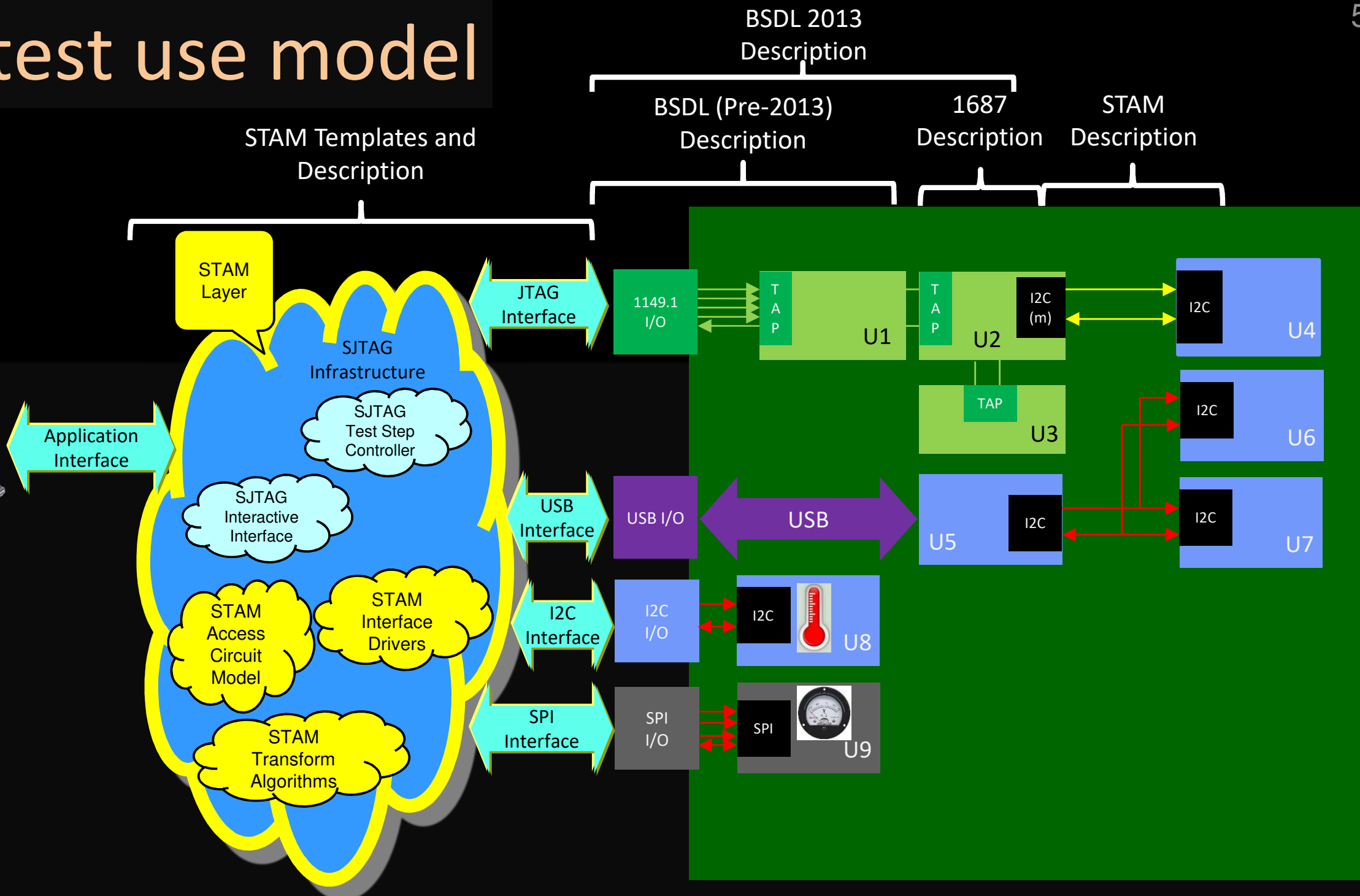
## IJTAG

- Internal JTAG, IEEE Std 1687
- [IEEE P1687.1](#)
- [IEEE P1687.2](#)

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# Board test use model

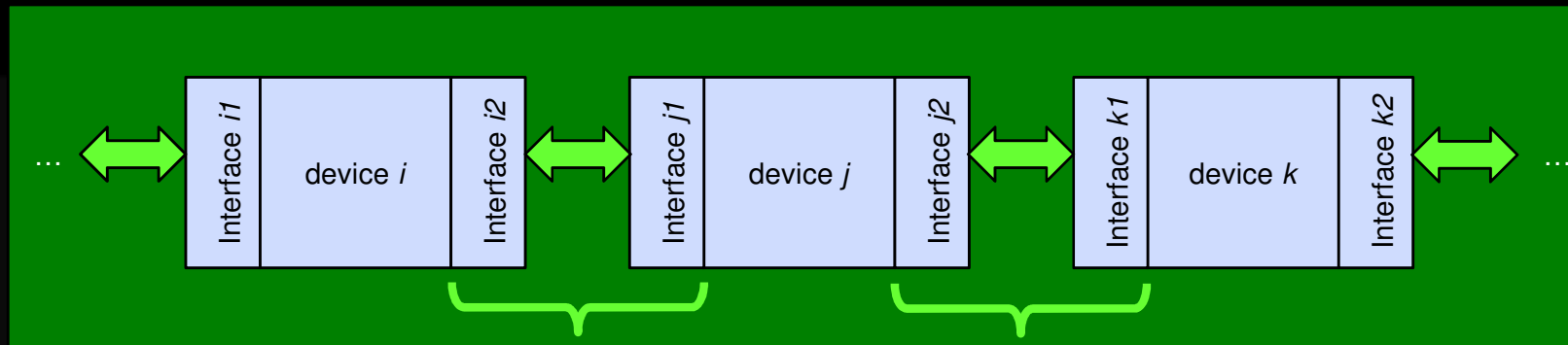


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# Transition points in the hierarchy

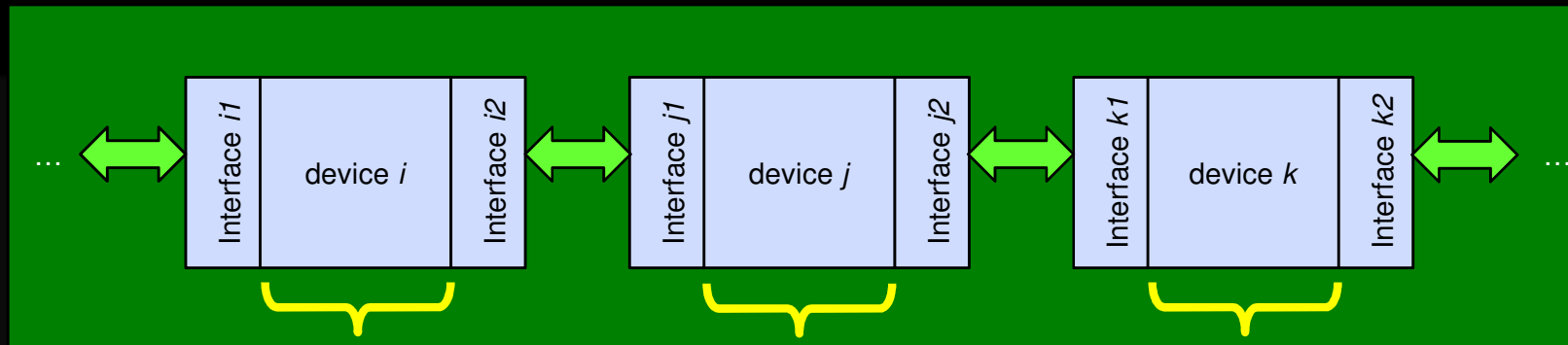
## Description



These are interface-to-interface connections using some defined protocol  
(e.g. I2C master to I2C slave)

# Transition points in the hierarchy

## Transformation



Device which (presumably) can transport data from one of its interfaces to another of its interfaces  
... but how? (example: USB RX -to- I2C master)

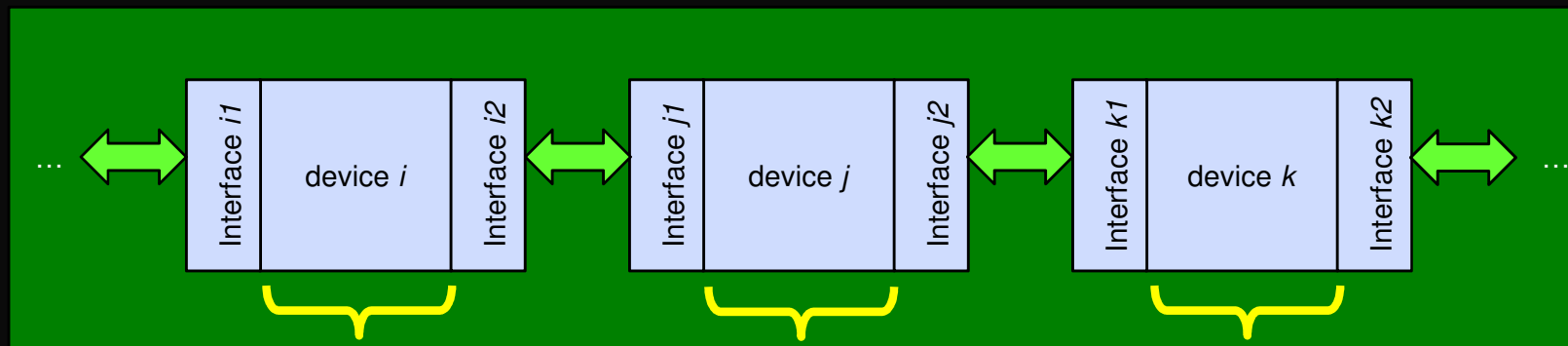
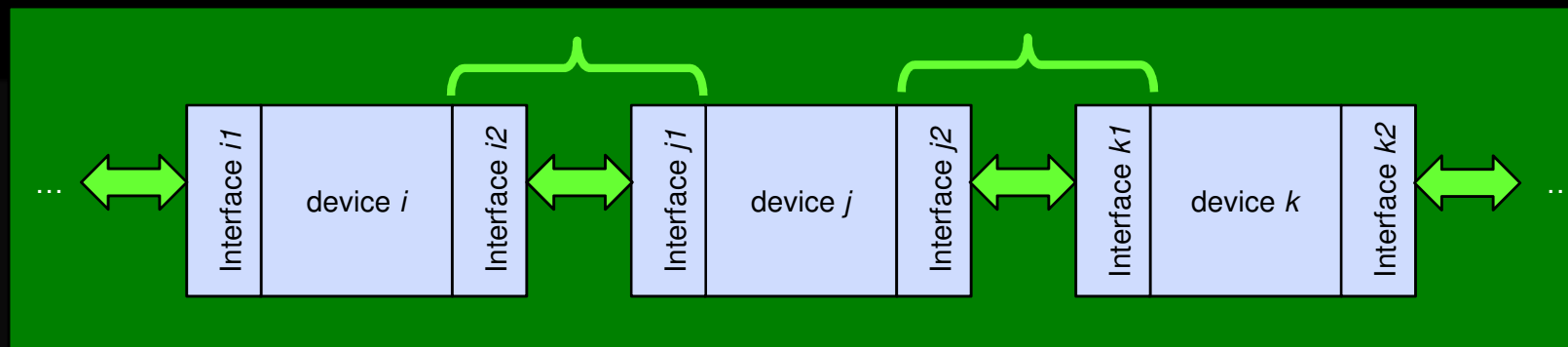


# Transition points in the hierarchy

P1687.1 scope may be kept narrow:  
presuming only that a DPIC can write the portal register.

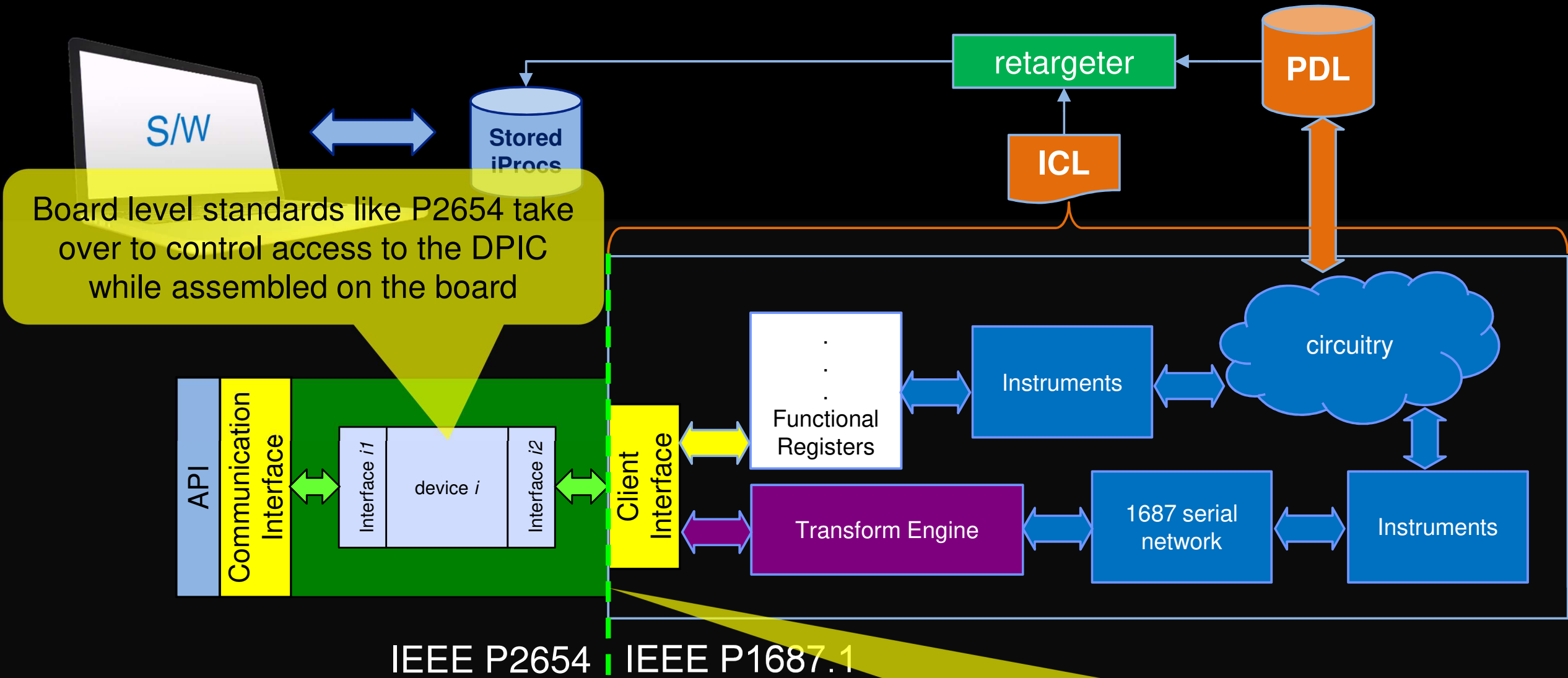
Which gives P2654 the more general problem  
to solve (from device pins to system edge).

## Descriptions



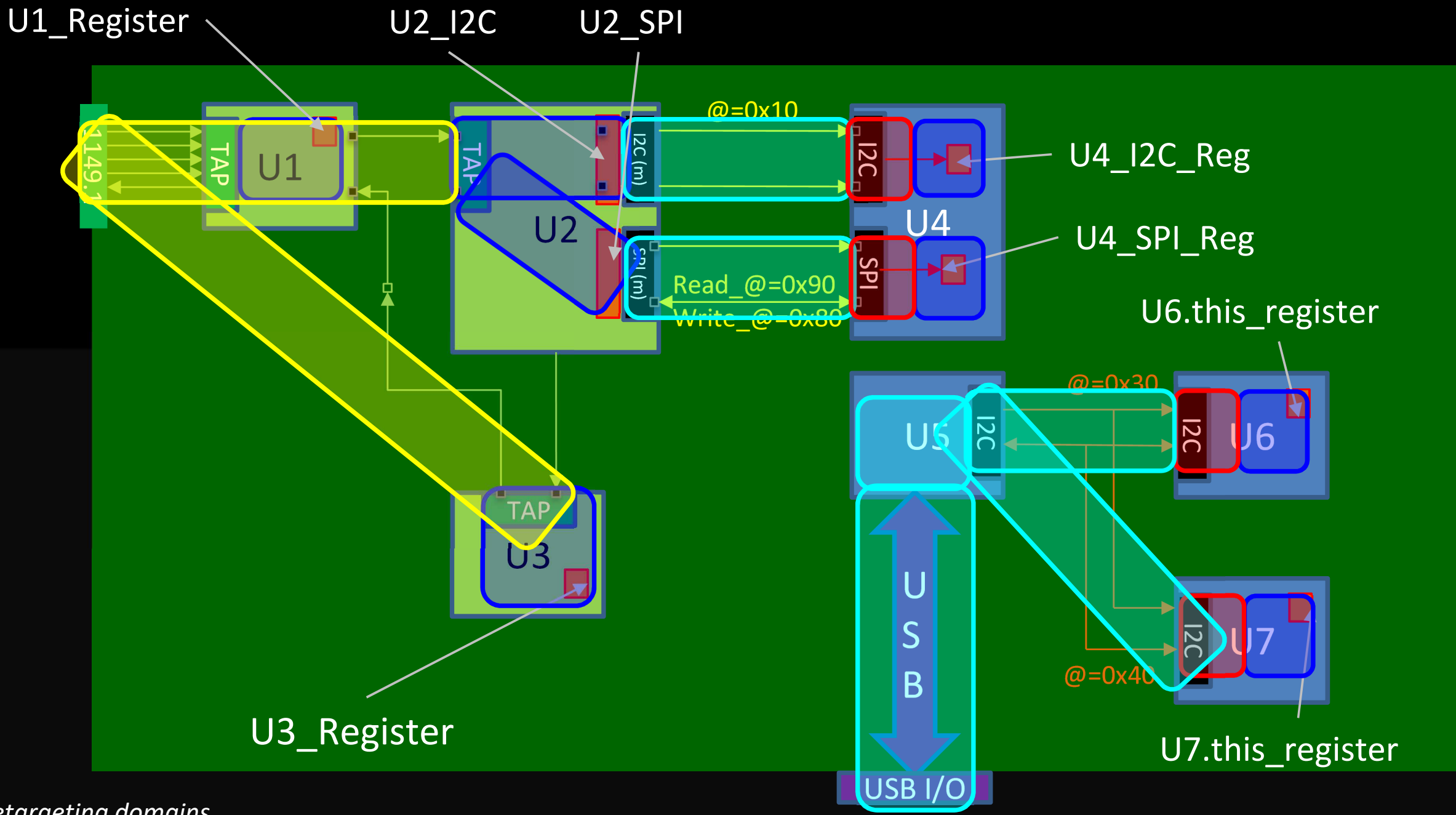
## Transformations

# Handoff Scope to Hierarchy



IEEE P2654 | IEEE P1687.1

P1687.1 ends at the DPIC Client Interface of the device



Legend: retargeting domains

1149.1

1687

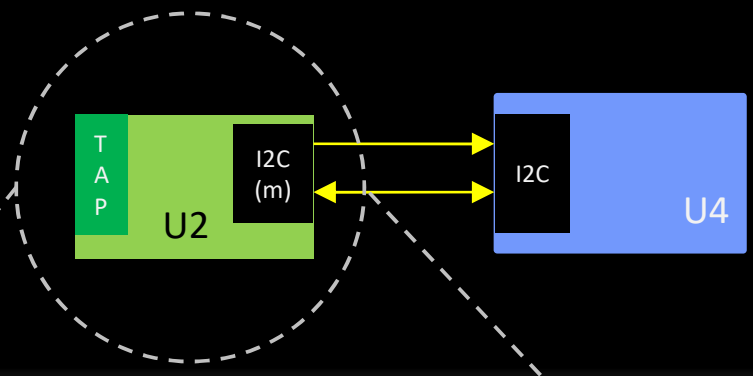
1687.1

SJTAG

# Outline

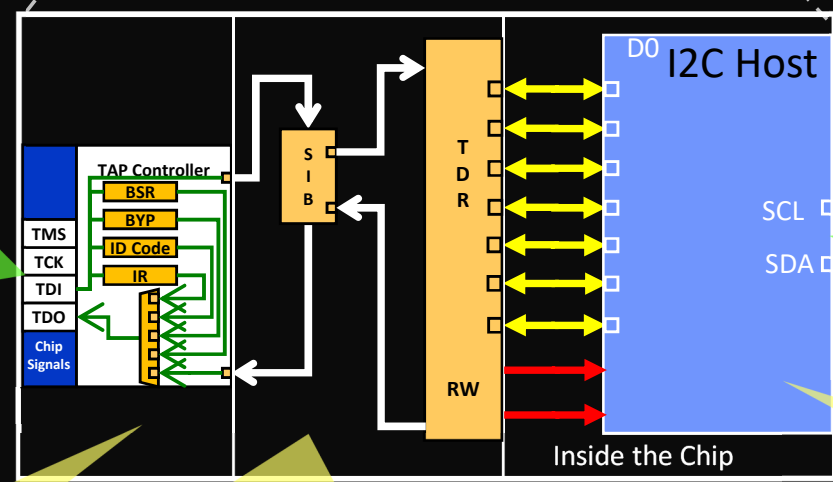
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# U2 JTAG to I2C Bridge Logic



Application has direct physical access to JTAG interface of U2. How to control interface to U4? *Via I2C Host in U2*

U2 needs to stimulate I2C interface to interact with U4, but application does not have direct control.



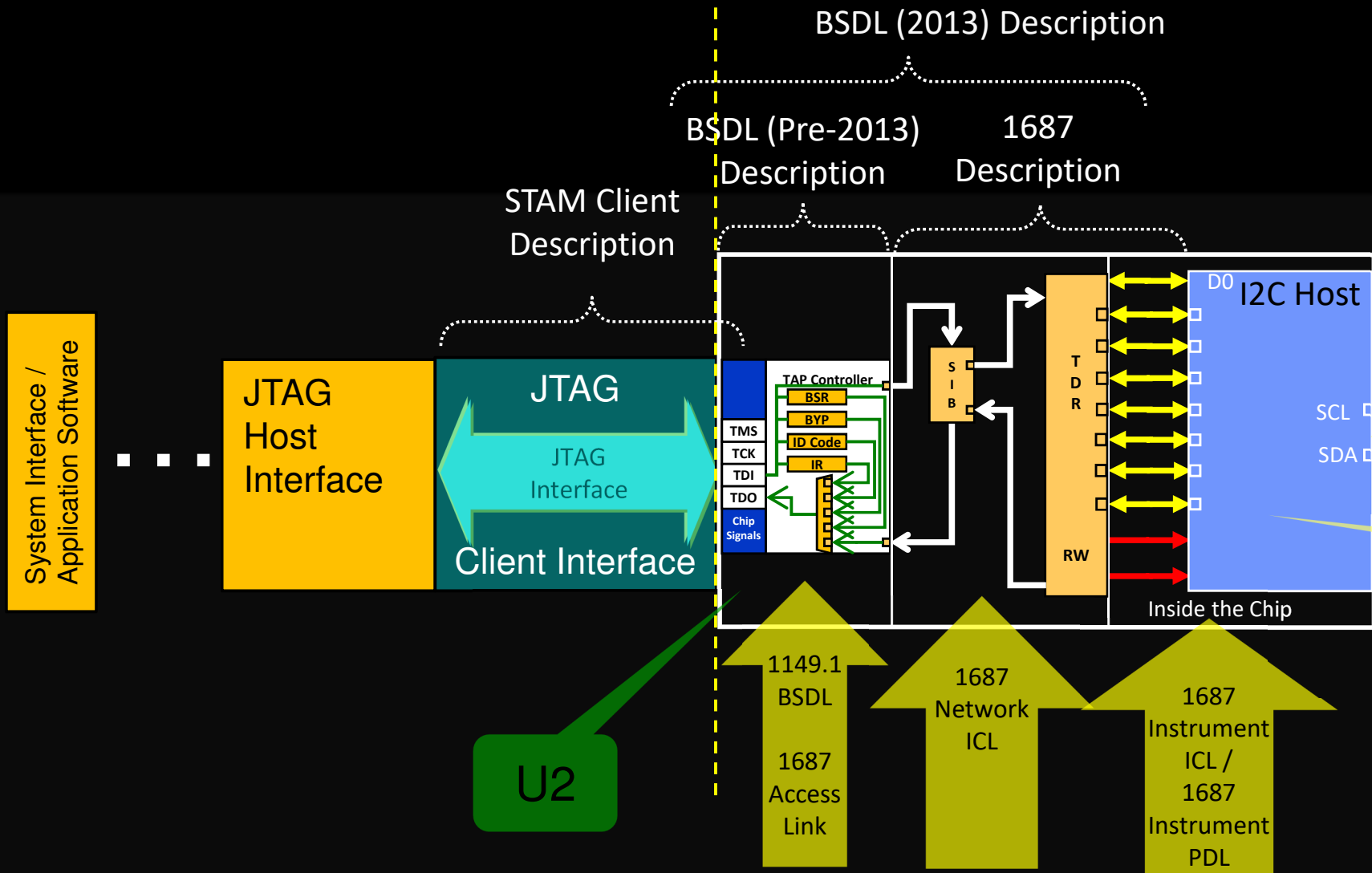
JTAG TAP Controller as STAM Client Interface from the application and board edge

Transformation Logic used to bridge control of I2C bus from JTAG bus

1687-based I2C Master as STAM Host Interface to U4 Client Interface

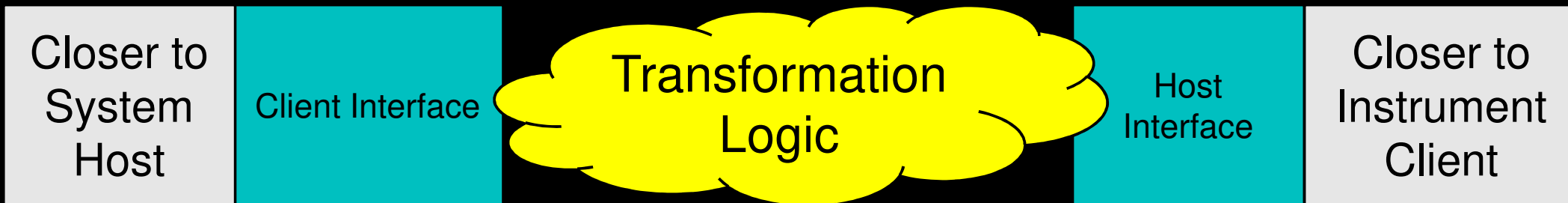
# STAM Generalized Bridge Model

STAM 1687 or 1149.1-2013

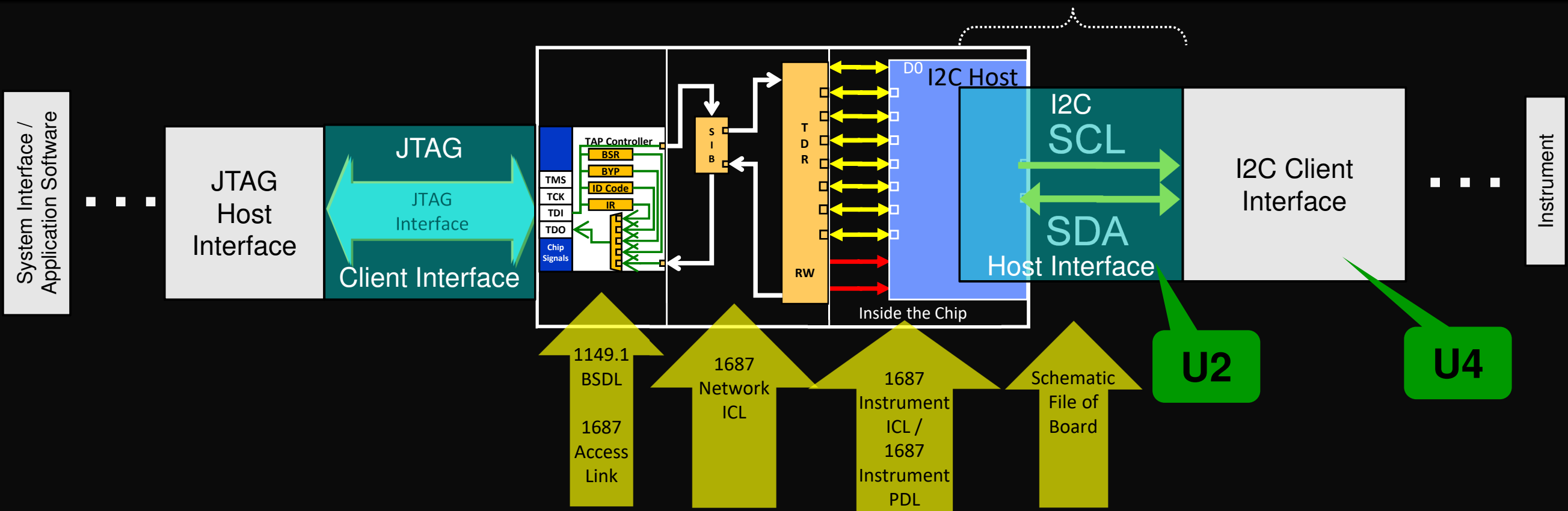


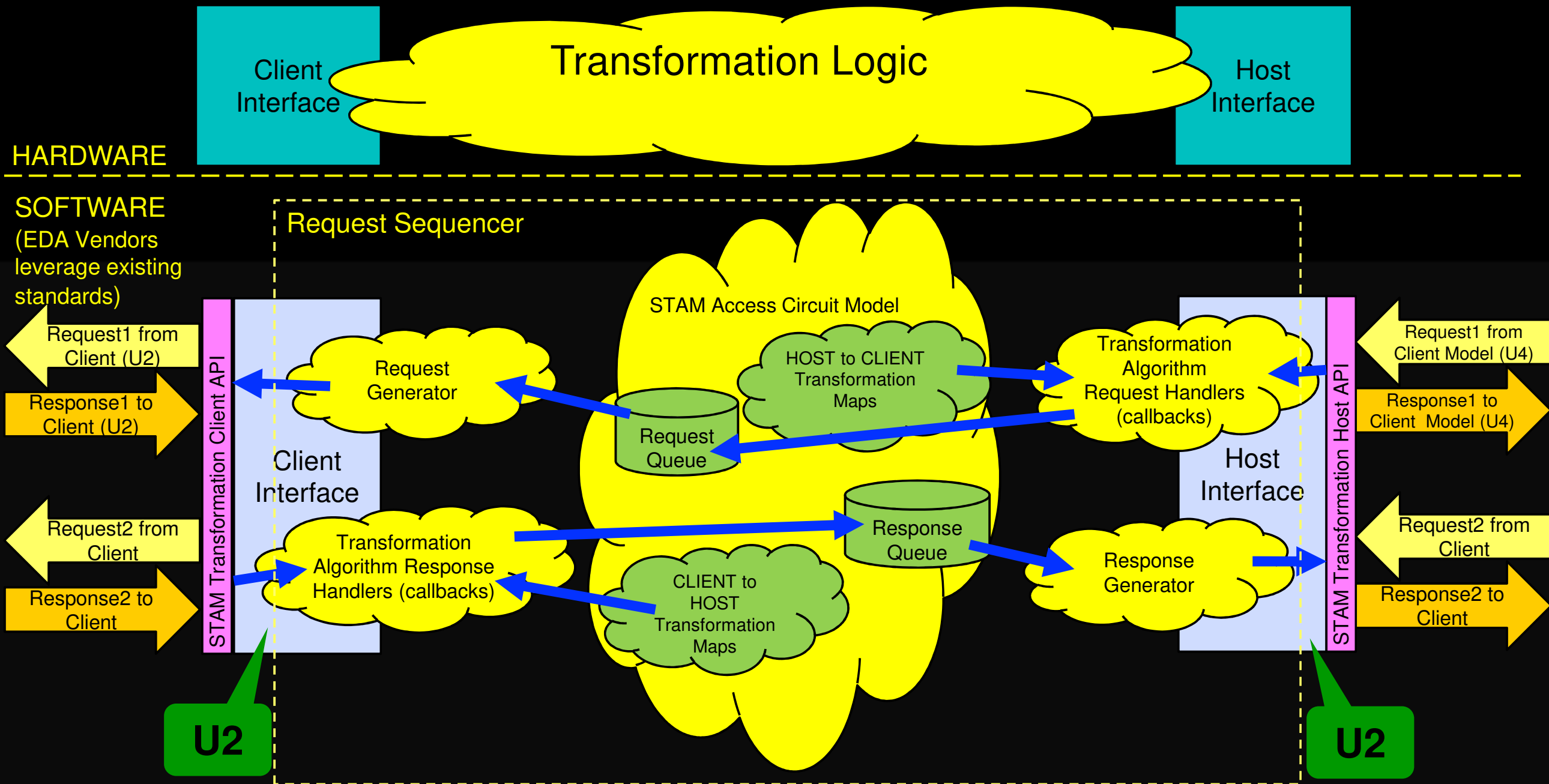
STAM provides access and control of I2C bus from JTAG to interact with clients connected to I2C bus

IEEE 1687 based Instrument (I2C Master)



STAM Host Description



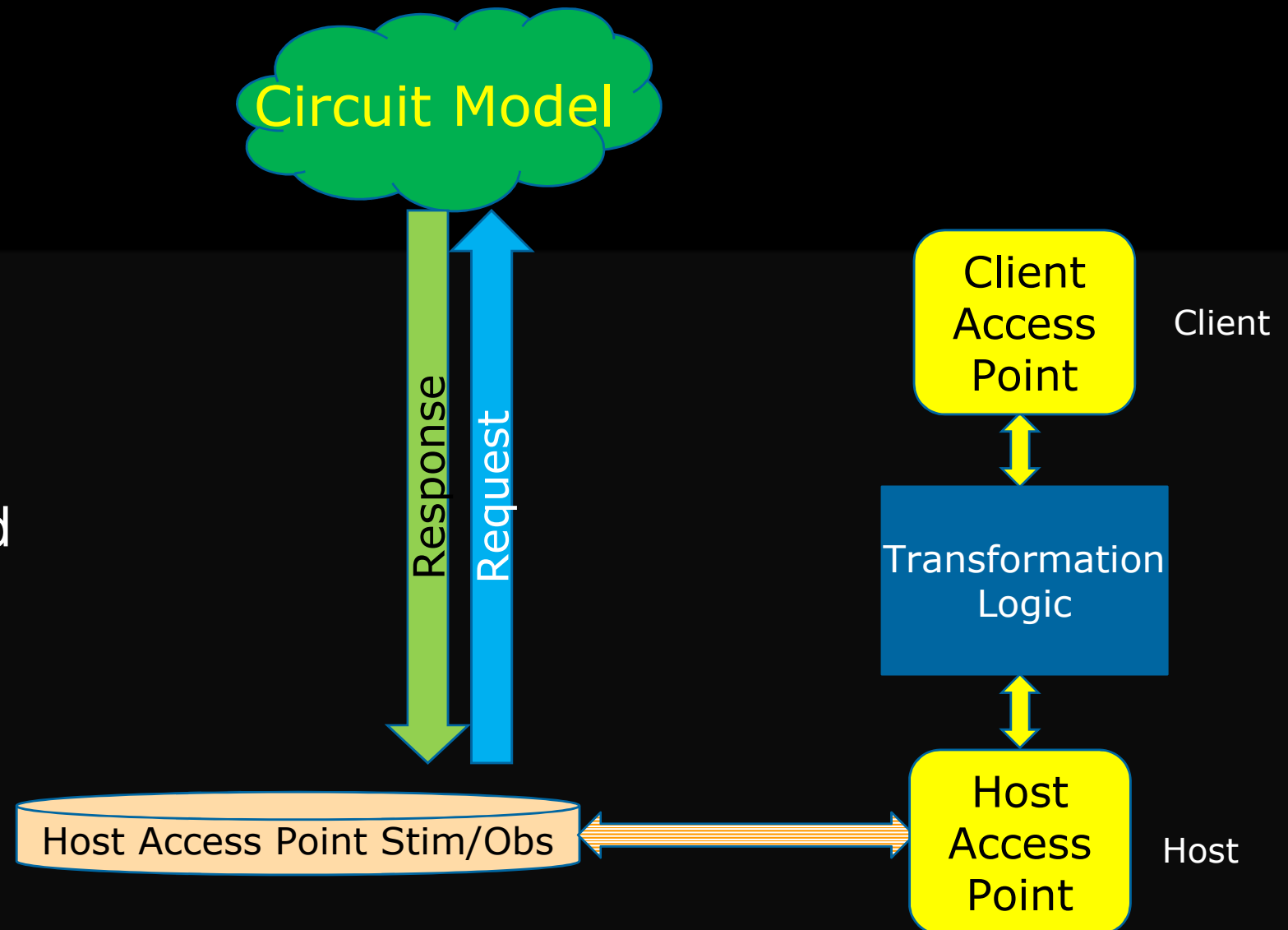




# Request and Response Model

(Bottom Up Approach Generalized)

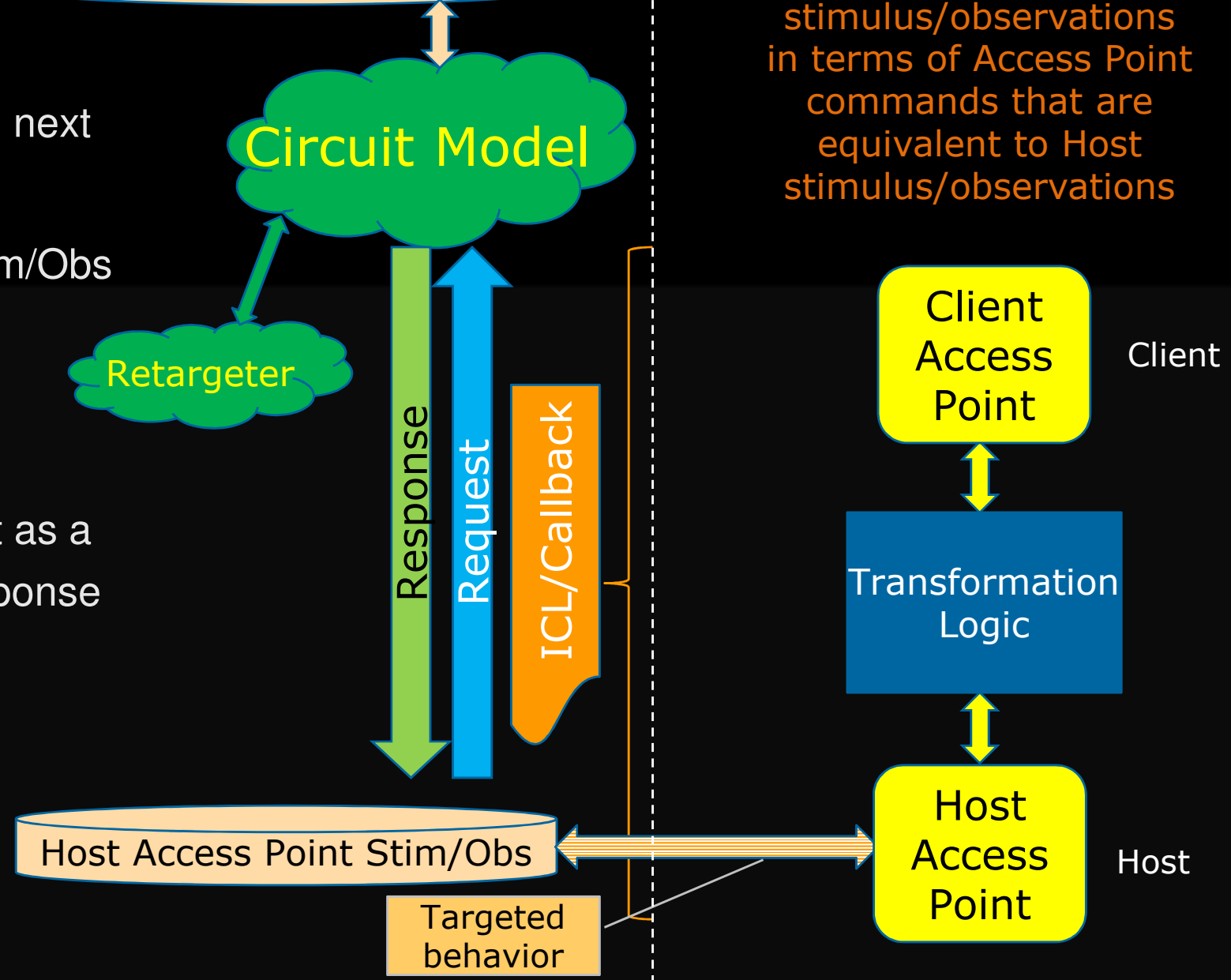
Analyzing hierarchical traversal of requests from instrument to top level interface, revealing transformation domains required at each level



Transformed Host Access Point Events that are to be applied as Client events to Client Access Point

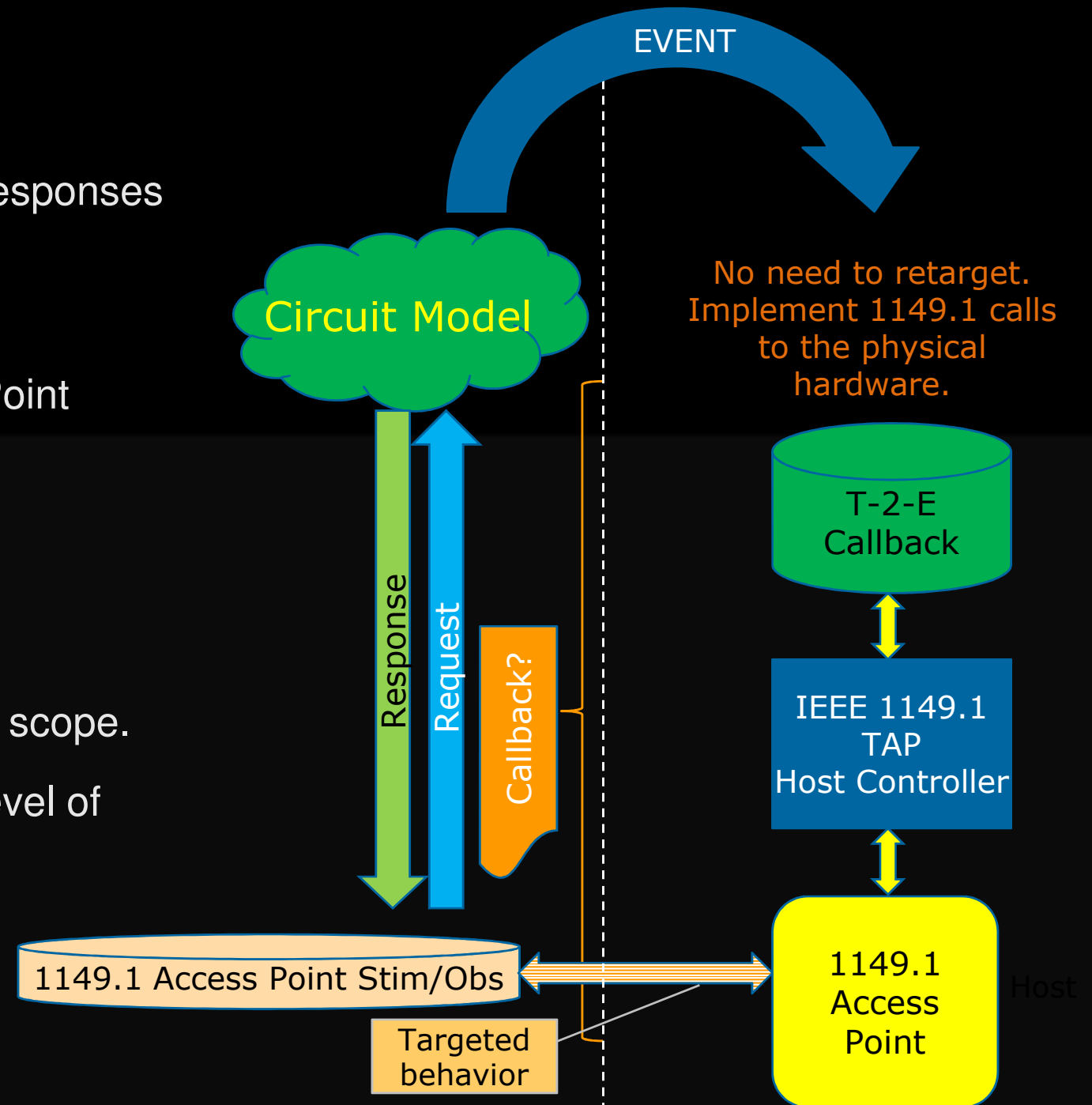
Ordered Collection of Access Point Stimulus/Observations for Client Access Point

- Host Stim/Obs define Requests/Responses required from next higher level
- Pass X: Request retargets Host Stim/Obs in terms of Client Access Point directive(s)
- Pass X: Response returns values observed at the Client Access Point as a result of a stimulus operation. Response is un-retargeted to Host scope.
- Instrument PDL is irrelevant at this level of retargeting: only interested in control of Host Access Point



Retarget: Need Client stimulus/observations in terms of Access Point commands that are equivalent to Host stimulus/observations

- 1149.1 Stim/Obs define Requests/Responses required from the next higher level
- Request translates 1149.1 Stim/Obs in terms of physical 1149.1 Access Point directive(s)
- Response returns values observed at the 1149.1 physical Access Point as a result of a stimulus operation. Response is un-retargeted to 1149.1 scope.
- Instrument PDL is irrelevant at this level of retargeting: only interested in control of 1149.1 Access Point



# Conclusions

- Efficient system level assembly test requires
  - Collaboration of domains/standards
  - Hierarchical support
  - Generalization to define behavior (not structure)
  - Transformation procedures to describe behavior of a particular hierarchical level

Visit [SJTAG.org](http://SJTAG.org) or [contact the authors](#) for a copy of this slide set