



SJTAG Backgrounder

The application of Boundary Scan within complex systems and an introduction to the SJTAG Working Group

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What is SJTAG?

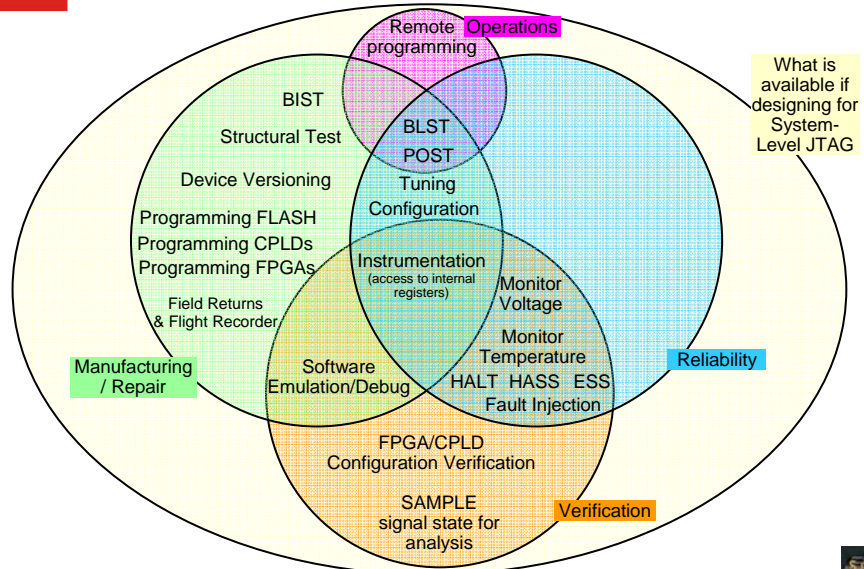
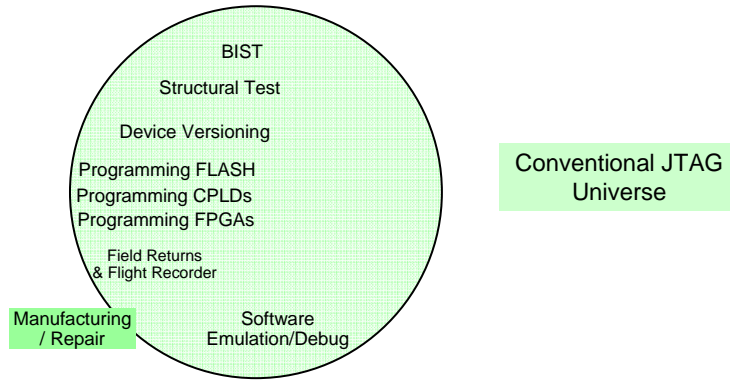


- **SJTAG :: System-level JTAG**
- **SJTAG refers to the use of IEEE 1149.1 based operations with assemblies consisting of multiple boards.**
- **SJTAG implies hierarchical structure that leverages the board level TAPs to enable system level activities**
- **SJTAG extends the scope of possible uses for JTAG to applications throughout the product lifecycle**
- **SJTAG accommodates both external and embedded Test Controllers and Test Managers (XBST and EBST)**

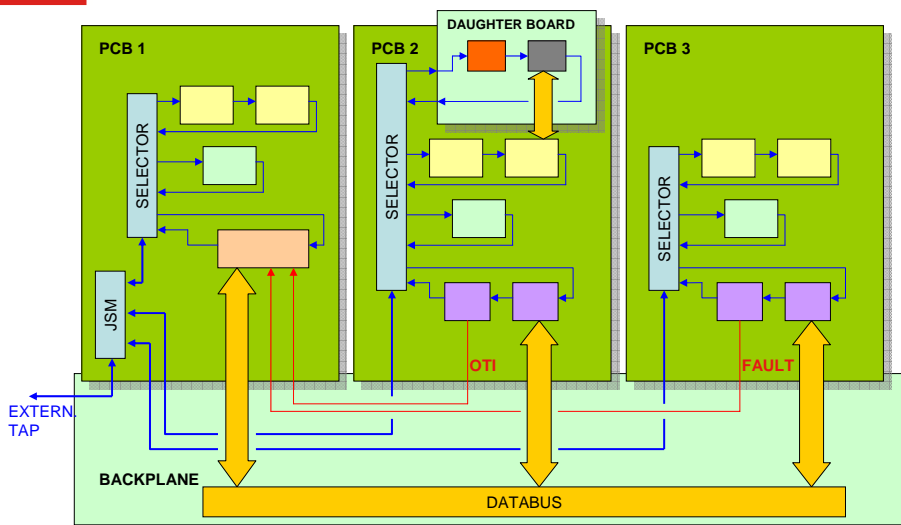
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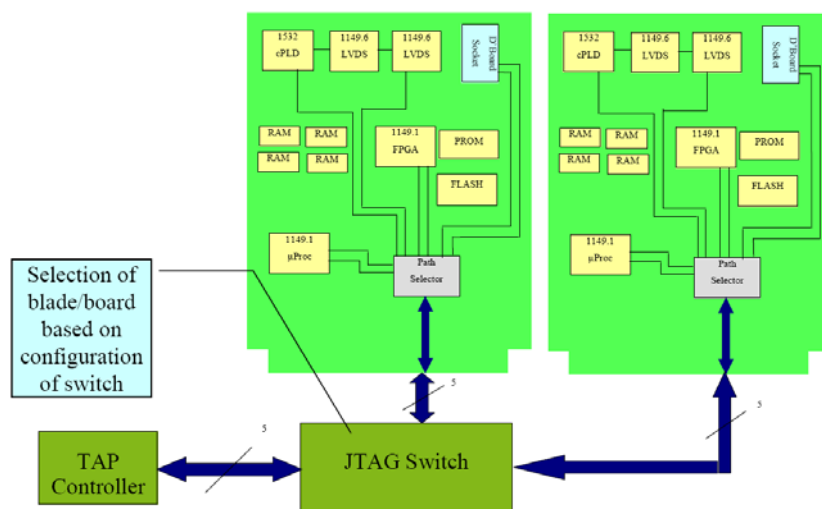


- **In general, scan chains resolve to a single TAP at the system level**
 - Need a means to select which board TAP to use.
- **TAP controllers may be embedded or external (or both!)**
 - Management of test execution, results storage and transfer, etc.
- **TAP voltage levels**
- **Boards are connected together (e.g. backplane)**
 - Opportunity to test interconnects between boards.
 - Need to control interaction between boards.
- **Boards within a system may be from multiple vendors**
 - Import/export of test/result vectors.
 - IP protection
- **Flexibility to elect not to install some boards**
 - Identification of system configuration

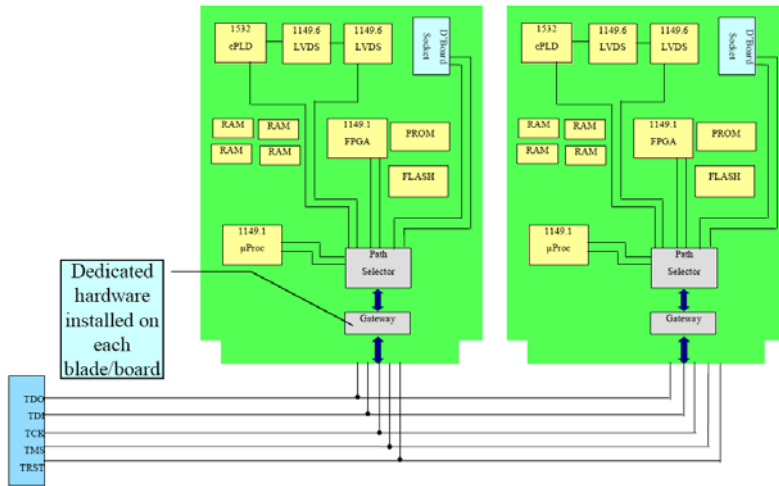


• Why should SJTAG be of interest?

- Compared to functional testing of a system, SJTAG offers:
 - Deterministic fault coverage
 - More detailed diagnostics (usually)
- In-field testing and re-programming possible with minimal equipment
 - Laptop and USB JTAG controller
 - Wireless remote access
- “Covers on” operations:
 - No disturbance to system configuration
- Systems level applications, such as:
 - Environmental Stress Screening/Testing (ESS/EST)
 - Software debugging/State capture
 - Fault injection
 - More...
 - Individual benefits may be small, but when taken together the overall value is much greater.



Multi-Drop Topology

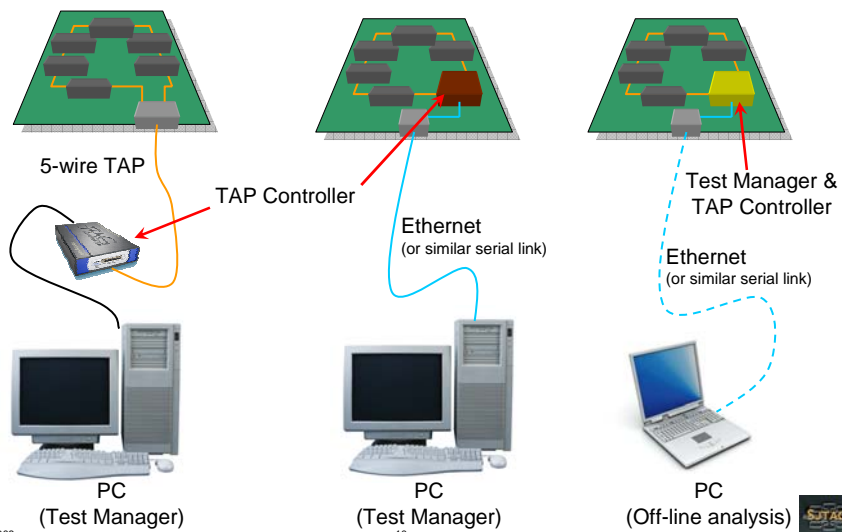


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XBST vs EBST



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Example: Radar Processor

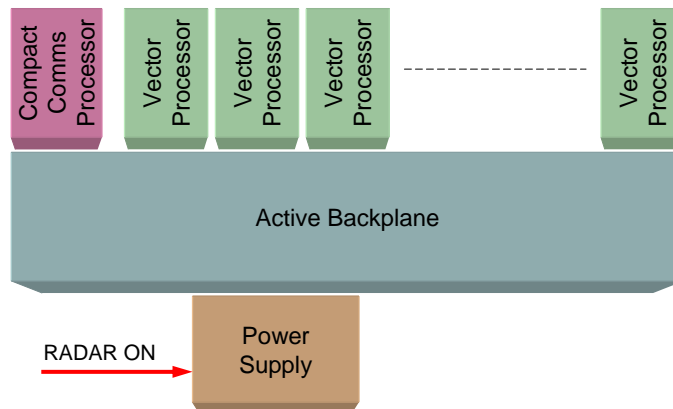


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Radar Processor Basic Architecture

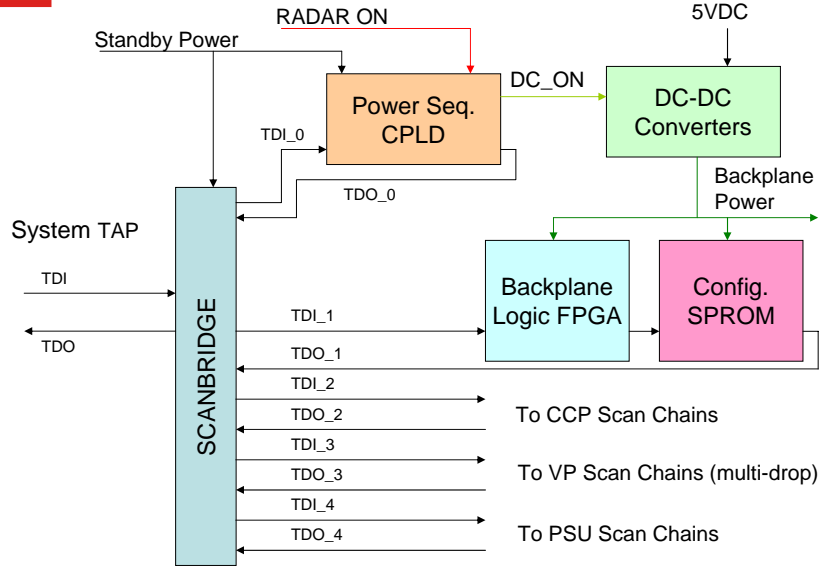


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Backplane JTAG Topology

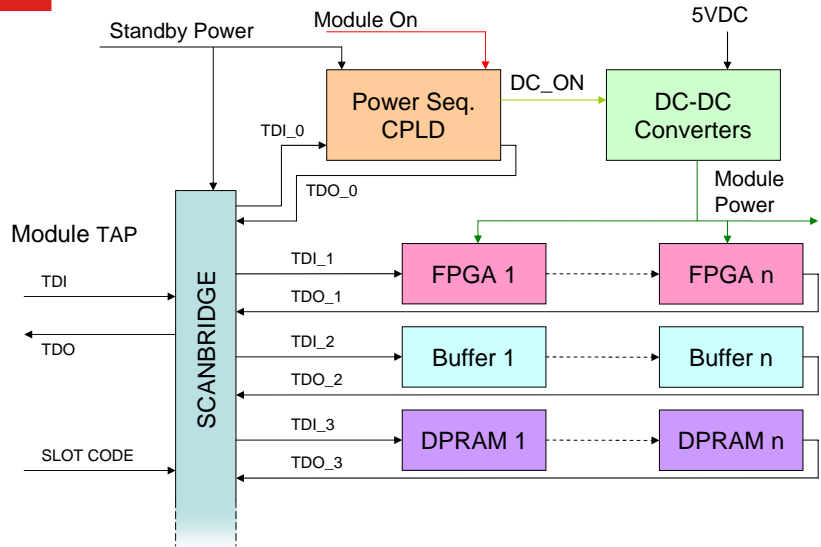


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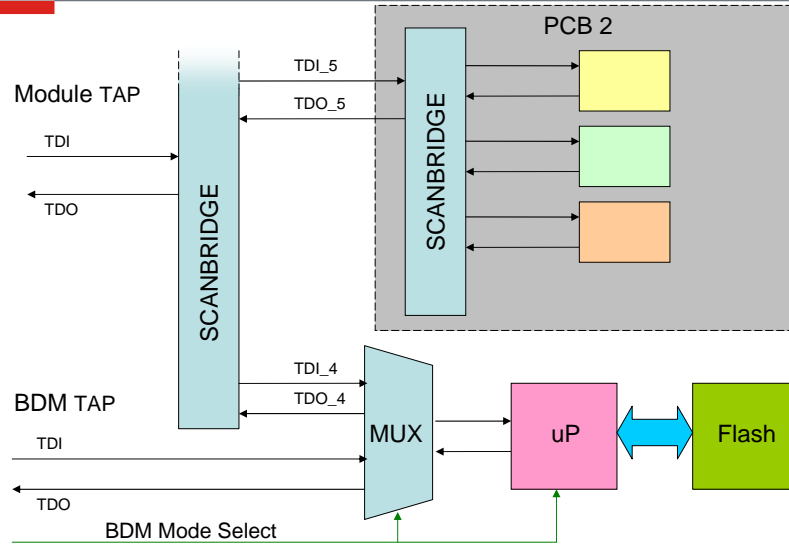
Module JTAG Topology (1)



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- **Reality is that it's not as simple as just connecting the boards with a scan chain linking device**
 - Not all the necessary information is in the CAD data
- **No single toolset supports all the possible applications**
 - Porting tests between vendors tools is not always easy
- **Many architectures are possible**
 - Tools may support some topologies but not others
 - Topology influences design of TAP interface to boards
- **Problems for the OEM vendor**
 - Data formats for exporting tests and results
 - Security – Protection of IP content in their design

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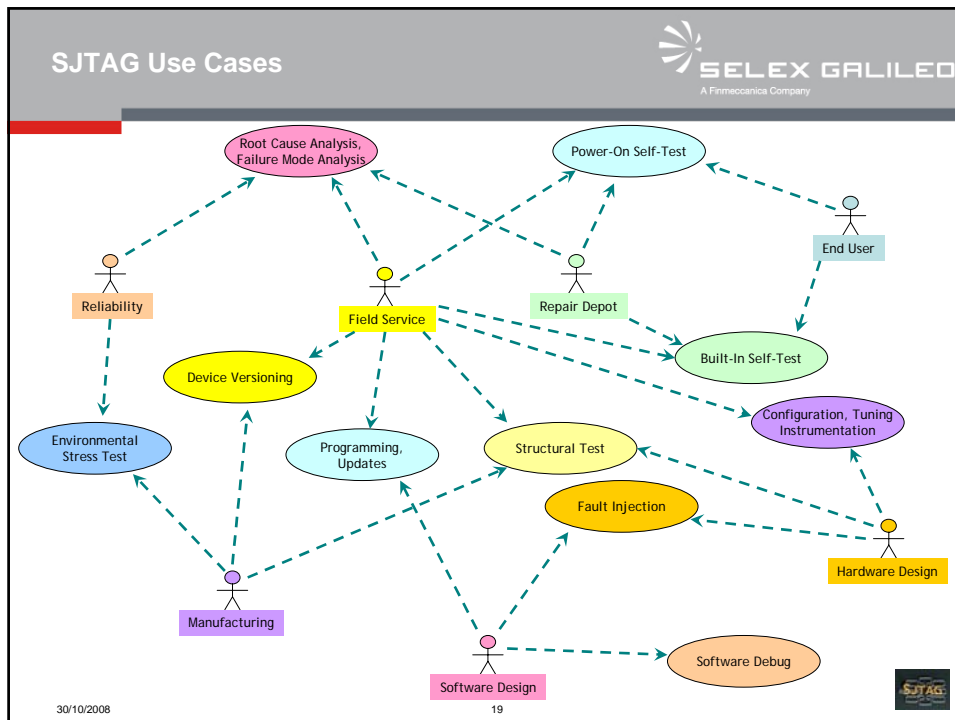


- **Formed in 2005 at the European Board Test Workshop**
- **Forerunner to the IEEE SJTAG Standard Working Group**
 - Scope and Purpose for IEEE PAR submission prepared
- **Preparing updated SJTAG White Paper**
 - 5 sections – “wiki” allows collaborative writing – <http://wiki.sjtag.org/>
 - Analyzing and Mining common methods/procedures/interfaces through use case analysis
 - Identifying minimum data sets required to support each Use Case
 - Working on value propositions for each aspect of the SJTAG Universe
 - Defining partitions/interfaces in both hardware and software architectures for standardization




- **Current Working Group membership includes representatives from:**
 - Device vendors
 - National Semiconductor; Firecron; Intellitech Corp.
 - Tool vendors
 - JTAG Technologies; GOEPEL Electronics; ASSET Intertech
 - EDA Vendors
 - Mentor Graphics; Cadence
 - End users
 - Ericsson; Alcatel-Lucent; Huawei Technologies; SAAB Aerotech; Cisco Systems; IBM; SELEX; Eastman Kodak
 - DfT Consultants
 - HDC AB; Integellus; DFT Solutions





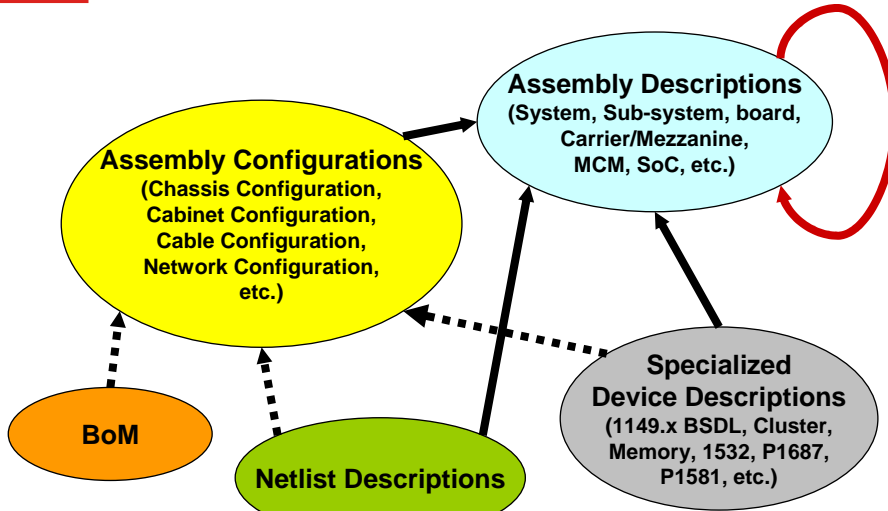
SJTAG Languages



SELEX GALILEO
A Finmeccanica Company

- **Existing JTAG related languages can be divided into three types:**
 - Those that detail the execution of a test or other JTAG operation (“canned vectors”) – SVF, JAM/STAPL
 - Those that help define the JTAG capabilities of a device or chain of devices – BSDL, HSDL
 - Those that describe the flow and control of a series of operations – Frequently tool vendor proprietary languages
- **But for system-level JTAG tooling to work effectively we also need:**
 - The structure/composition of the system – could be dynamic
 - Constraints – possible reset conditions, contentions
 - **Not everything is available from the CAD data!**

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- **Weekly meeting by conference call**

- One-hour discussion – main topics decided in advance by chair.
- Occasional “live” meetings, usually at conferences such as VTS or ITC.

- **On-line presence**

- SJTAG website provides access to meeting minutes, documents and presentations, and on-line discussion forum:
<http://www.sjtag.org/>
- Monthly newsletter for members and “fringe observers”



- **It is a principle of the IEEE that anyone can contribute to, or comment on, the development of IEEE standards**

- The SJTAG Working Group believes it one of the most open and accessible groups currently operating
- Documents, presentations and meeting minutes are available from the SJTAG website
- You can self-register to use the discussion forums or add to the Wiki – **you do not have to be a member of the Working Group**
- If you do want to join the Working Group and play an active role, then contact us through the website



