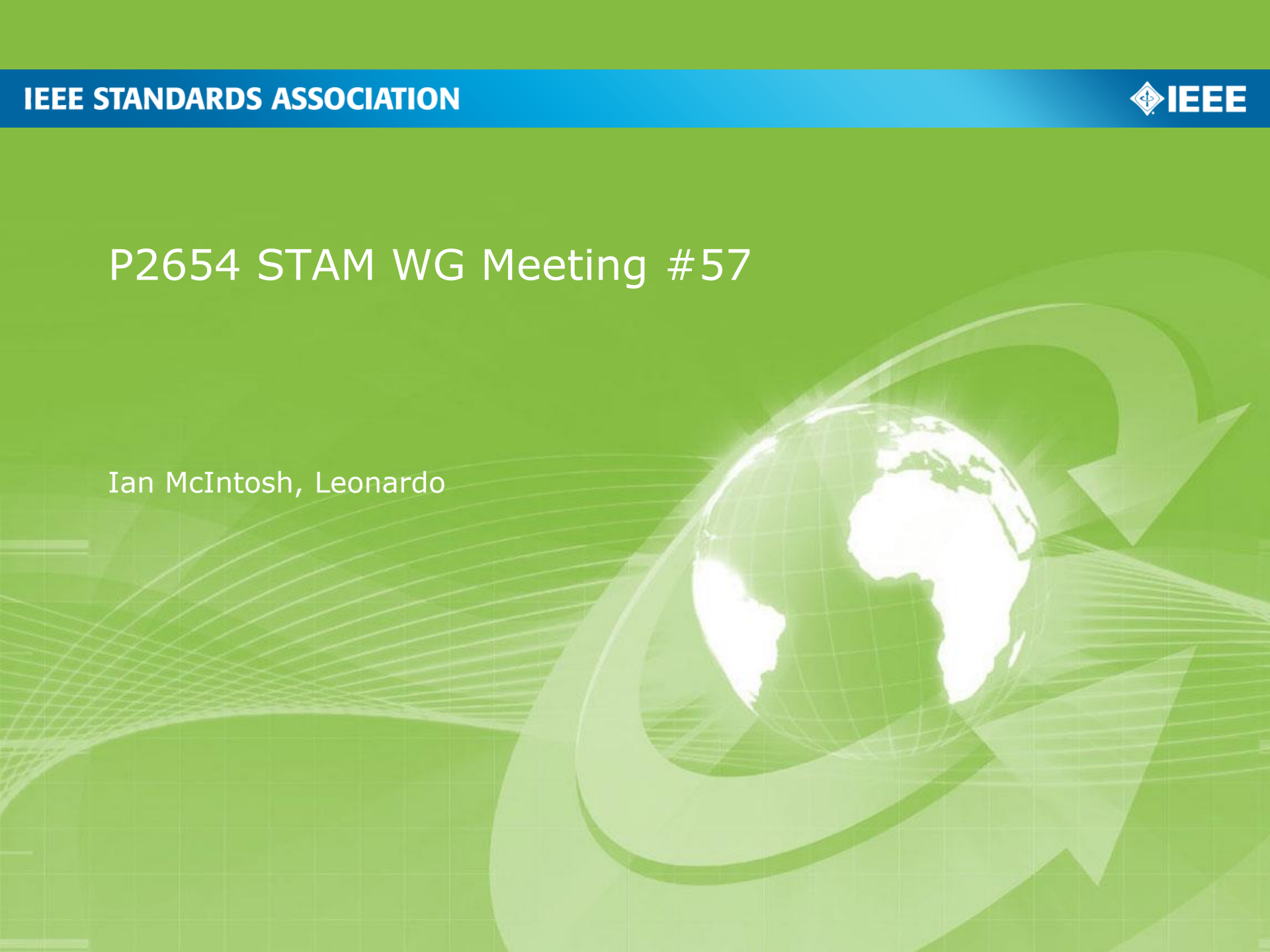
P2654 STAM WG Meeting #57

Ian McIntosh, Leonardo



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IEEE P2654
System Test Access Management
Ian McIntosh (chair)

Working Group Meeting #57			
Date: 2020-03-09			
Author(s):			
Name	**Affiliation**	**Phone [optional]**	**Email [optional]**
Ian McIntosh	Leonardo		

2. Agenda

1. Roll Call
2. Agenda
3. IEEE Patent and Copyright Slides
4. Review and approve previous minutes: March 2
5. Review open action items
6. Inter-group Collaboration
7. Discussion Topics:
    a. Continue on outline of the draft: Assembly of assemblies, "system" definition
    b. Use Cases: Intent and objectives
8. Any other business
9. Key Takeaways from today's meeting
10. Glossary terms from this meeting
11. Schedule next meeting
12. Topic for next meeting
13. Reminders
14. List new action items
15. Adjourn

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- **Cause an LOA to be submitted to the IEEE-SA (patcom@ieee.org); or**
- **Provide the chair of this group with the identity of the holder(s) of any and all such claims as soon as possible; or**
- **Speak up now and respond to this Call for Potentially Essential Patents**

If anyone in this meeting is personally aware of the holder of any patent claims that are potentially essential to implementation of the proposed standard(s) under consideration by this group and that are not already the subject of an Accepted Letter of Assurance, please respond at this time by providing relevant information to the WG Chair

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      - Technical considerations remain the primary focus
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  - Don't be silent if inappropriate topics are discussed … do formally object.

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The patent policy and the procedures used to execute that policy are documented in the:

- *IEEE-SA Standards Board Bylaws*
  (http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#6)
- *IEEE-SA Standards Board Operations Manual*
  (http://standards.ieee.org/develop/policies/opman/sect6.html#6.3)

Material about the patent policy is available at
http://standards.ieee.org/about/sasb/patcom/materials.html

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- The **IEEE-SA Copyright Policy** is described in the *IEEE-SA Standards Board Bylaws* and *IEEE-SA Standards Board Operations Manual*
  - IEEE-SA Copyright Policy, see
    Clause 7 of the *IEEE-SA Standards Board Bylaws*
    https://standards.ieee.org/about/policies/bylaws/sect6-7.html#7
    Clause 6.1 of the *IEEE-SA Standards Board Operations Manual*
    https://standards.ieee.org/about/policies/opman/sect6.html

- IEEE-SA Copyright Permission
  - https://standards.ieee.org/content/dam/ieee-standards/standards/web/documents/other/permissionltrs.zip
- IEEE-SA Copyright FAQs
  - http://standards.ieee.org/faqs/copyrights.html/

- IEEE-SA Best Practices for IEEE Standards Development
  - http://standards.ieee.org/develop/policies/best_practices_for_ieee_standards_development_051215.pdf

- Distribution of Draft Standards (see 6.1.3 of the SASB Operations Manual)
  - https://standards.ieee.org/about/policies/opman/sect6.html

4. Review and approve minutes

Working Group Meeting #56, March 2

Draft circulated March 2.

Attendees:

Ian McIntosh (Leonardo)
Eric Cormack (DFT Solutions)
Terry Duepner (National Instruments)
Heiko Ehrenberg (GOEPEL Electronics)
Brian Erickson (JTAG Technologies)
Peter Horwood (Digital Development Consultants Ltd)
Bill Huynh (Marvell Inc.)
Joel Irby (AMD)
Richard Pistor (Curtiss-Wright)
Jan Schat (NXP Semiconductors)
Naveen Srivastava (Nvidia)
Jon Stewart (Dell)
Louis Ungar (A.T.E. Solutions)
Brad Van Treuren (VT Enterprises Consulting Services)
Carl Walker (Cisco Systems)

5. Review open action items

Action Item Register:
http://files.sjtag.org/PostStudyGroup/ActionItemRegister.xlsx

Format of action number is
[Meeting#.Action# within that meeting]

[38.1] Brad: Email brief instruction on using the simulation tool.

- Starting on documentation, possibly ready in coming weeks.

[56.1] Brad to request "LoA in principle" from Michele.

6. Inter-group Collaboration

News and updates from other standards groups.

- Officer elections from other groups:

	P1500	P1687.2	P2427
Chair	Mike Ricchetti	Stephen Sunter	Stephen Sunter
Vice-chair	Grady Giles	Vladimir Zivkovic	Salem Abdennadher
Secretary	Ben Niewenhuis	Hans Martin von Staudt	Devanathan Varadarajan
Editor	Paul Reuter	Jeff Rearick	Anne Meixner

7. Discussion Topics

7.a Continue outline of the draft (Assembly of assemblies, "system" definition)

- Resources:
  - Microsoft Word Template: https://development.standards.ieee.org/myproject/Public/mytools/draft/wordtemp.zip
  - Style Manual: https://development.standards.ieee.org/myproject/Public/mytools/draft/styleman.pdf
  - Document Brainstorming notes moved to separate pack for reference: http://files.sjtag.org/P2654WG/P2654_Reference_Pack.pptx
  - Forum thread: http://forums.sjtag.org/viewtopic.php?f=3&t=829
  - Draft Outline WIP at end of this pack

7.b Use Cases: Intent and Objectives

- What will we do with them?; How will it benefit the standard?

Wrap-up items

8. Any other business
9. Today's Key Takeaways
10. Glossary terms from this meeting
11. Schedule next meeting
    - March 16
12. Topic for next meeting
    - TBD
13. Reminders
14. List new action items
15. Adjourn

January 6 Section Headings

DRAFT OUTLINE

Draft Outline

1. Overview
2. Normative references
    1. IEEE Std. 1149.1-2013 etc.
3. Definitions
4. Concepts and Architecture/Technology (Small introduction of points/concepts)
    1. Introduction
    2. Relationship to other standards
    3. Interfaces
        1. Physical Layer (leveraged standards)
        2. Access and Data Link Layer
    4. Software Model
    5. Transformational Logic
    6. Retargeting
    7. Order of execution of commands
    8. Synchronization across interfaces
    9. Impediments
    10. Test Portability
    11. Security

Draft Outline (Continued 1)

5. Interfaces
    1. Physical Layer (leveraged standards)
        a) Formal standards (IEEE 1149.1, 1687, 1500, etc.)
        b) Proposed standards (IEEE P1687.1, P1687.2, P1149.7, etc.)
        c) Industry standards (I2C…, SPI, etc.)
        d) Ad hoc standards compliance via generic interface description (callbacks)
    2. Access and Data Link Layer
        a) Description of Access Link
        b) Description of Data Link
        c) Callbacks
        d) Retargeting for Access Link
        e) Illustration of concept
    3. Hand-off/Relation to other standards
        a) API vs. Streaming packet (function call vs. iSCSI message method) Why decision for method?
        b) Hand-off discussion
        c) Format of data messages (reference Software Data Model)
        d) Illustration of concept

Draft Outline (Continued 2)

6. Software Model
    a) Data Format shared between modules
        i. Detail the format used for messages between modules
    b) Circuit Description (how transformations interface)
        i. Something in the order of ICL and PDL as a descriptive language
    c) Transformation Description (the transform algorithm)
        i. How to get from point A to point B
            a. General transformation concept
            b. Retargeting impact
            c. Leveraging other standards as part of the transformation (e.g., JTAG to I2C Bridge where I2C Host is described with IEEE 1687)
    d) Structural Model
        i. How entities are wired together
            a. Netlist – Minimal topological information (interfaces) required (ex. Like what AI did with HSDL)
            b. Description of interfaces
            c. Etc.
        ii. Model components
            a. Transformation Maps
            b. Request Queues
            c. Response Queues
            d. Handlers (Callbacks)

Draft Outline (Continued 3)

7. Operational Overview
    a) Hierarchical Modules (Client to Host relationships)
        i. Describe a single module concept (like slides in presentations)
        ii. Describe role of client interface
        iii. Describe role of host interface
        iv. Software dependencies
            a. Host and Client Interfaces define the entry points to the module
            b. These interfaces have dependency on handlers being available to decode the messages through the interfaces
            c. The handlers have dependency on the model data for both configuration and state capture of hardware state for synchronization between software model and actual hardware entity
        v. Hint to description language format?
        vi. Definition of the P2654 host and client interface abstraction
            a. Message interface or do we use a class API to describe it (message with command code in header vs. a function/method described in the description language as the reference to what handler to call)
    b) Hierarchical Relationships
        i. Reliance on retargeting of host within bridge devices
        ii. Dynamic configuration of the path to open all AccessLinks to the target instrument. Do we want this to be automatic by the tooling or specified by the user as part of the algorithm?

Draft Outline (Continued 4)

8. System Concepts (More Detailed Descriptions)
    a) Assembly of Assemblies (vs discrete system, board, device, core)(connectivity is what matters)(Need to prevent pigeon hole one type from an aggregation – 16TB aggregate of 16-1TB memories)(Sub- reveals hierarchy)(Not using Sub- allows for pure aggregation and recursive nature relationship)(hierarchy vs. recursion)(Recursion – same thing/interface at various levels of the hierarchy)(SALT/NaCl – testing of SALT not Na and Cl separate necessarily)(STAM interested in stimulus and response not the function of the system. That is outside our scope.)
    b) Spanning across physical boundaries (cable interfaces)
    c) Need simple diagrams of concepts
    d) Multi-drop vs. point to point vs. switch/router
    e) Available resources from sub-assembly? Discovery Activity
        i. Is this in STAM scope? Brought up multiple times.
        ii. Do we not support systems with subassemblies? We need discovery for sub-assemblies.
        iii. Is this an extended discovery feature: Dynamic query vs. static description in model. Absolutely need to have static discovery.
        iv. This is a discriminator between P1687.1 and P2654. P1687.1 deals bottom up with PDL. P2654 has some top down discovery needs.
        v. How does this relate with retargeter? Manually (separate) or integrated.

Draft Outline (Continued 5)

8. System Concepts (More Detailed Descriptions)
    f) Available test targets
        i. Registers or Registers and 1687 ports (signals)
        ii. Overloading of term port: Port != port – Signal vs. I2C Address
        iii. IEEE 100-2000 Dictionary Port: port
            1) (1) (electronic devices or networks) A place of access to a device or network where energy may be supplied or withdrawn or where the device or network variables may be observed or measured. Notes:
                1. In any particular case, the ports are determined by the way the device is used and not by its structure alone.
                2. The terminal pair is a special case of a port.
                3. In the case of a waveguide or transmission line, a port is characterized by a specified mode of propagation and a specified reference plane.
                4. At each place of access, a separate port is assigned to each significant independent mode of propagation.
                5. In frequency changing systems, a separate port is also assigned to each significant independent frequency response.
            2) (10) An interface point connecting a communications channel and a device.
            3) (12) A conceptual point at which a cell or a hierarchical design unit makes its interface available to higher levels in the design hierarchy.
    g) Testability targets can be a feature. Realize functionality alone may not be ideal for a test application (e.g., BIST may require constraints, Signal generator may require a narrow range with higher resolution than factory test. BIST may only test a few frequencies that are not the same ones used in your application.)

Draft Outline (Continued 6)

~~9. Compliance~~/Conformance Concepts (Compliance Verification?) [Maybe move as last chapter before annex]

- ~~a) Degrees of~~ compliance vs compatible
- b) Compliance conforms to all essential rules of standard
- c) Compatible complies with some rules of standard to allow communications
- d) Must haves (mandatory), nice to have (recommendations, extension), can't do it(?)
- e) Black box support: Provisions for inputs that perform a particular response in the HW pins with stimulus
  - a) Discovery/declaration
  - b) Data in on digital interface – waveform on analog interface (example)
  - c) PDL like procedures supplied by the black box vendor
  - d) Discovery requires low level entity to supply something like a PDL procedure (e.g., by reference vs explicit)

Draft Outline (Continued 7)

10. Extended Concepts (How to plug into STAM)
    a) Perspective of view
    b) Leveraging lower level (standards or ad hoc)
        i. What an interface definition/specification needs to provide
        ii. Hand-off criteria
    c) Transformation reference between modules
        i. Data tracking (what bits are important)
        ii. Sequential vs. cached or queued processing of requests and responses (behavioral options)
    d) Hierarchies
        i. Scalability
        ii. Attributes – configurations?
        iii. Task assignments – Division of tasks
            i. High level – application
            ii. Single Test Sequence
            iii. Single Test Step
            iv. Instrumentation – Spectrum Analysis, Voltage Monitor, Power Supply, etc.
            v. Low level primitive
    e) Difference in stimulus/data
        i. Set up with digital stimulus and measure with analog output
        ii. Cluster tests (diagnostics inside cluster of logic accessible with stimulus and observation surrounding its boundary)
        iii. Tx/Rx loopback testing from DAC to ADC
            a. Requiring manual intervention to define stimulus and how to interpret observed

Draft Outline (Continued 8)

11. Advanced Concepts (Interesting but different use cases)
    a) System Interface (message based stream)
        i. STAM message packets over product communications interfaces
        ii. Queries of services available
        iii. Proxy (indirect test bus control via another interface) Interface
    b) System of Systems (complex perspective)
        i. How does this differ from 10.d Hierarchies
        ii. Racks of shelves of blades
        iii. Collections of LRUs
        iv. Interconnected by cable assemblies/harnesses
        v. Smart cables?
        vi. System (has a brain/CPU?)
        vii. System (able to operate autonomously)
        viii. Can we qualify what a system is in terms of being able to identify what can be replaced to make "System" operational again? How deep down do you go?
        ix. Repairable devices vs. soft repair of device (redundancy) – still need to mark as reduced availability

Draft Outline (Continued 9)

I. Education (Place holder about how to use and examples)
   a. Rule
   b. Permissions
   c. Preventative measures to ensure compliance
   d. Timing impact due to complexity of hierarchical interface

January 6 and 13 suggestions

CANDIDATE USE CASES

Use Cases

- TDR access between two end points
  - Interconnect Test between two end points
- SerDes Test between two end points
  - Same domain (IEEE Std. 1149.1-2013)
    - Device to Self
  - Different domain (IEEE Std. 1149.1-2013 and IEEE Std. 1687-2014)
    - Device to Device
    - Device to ATE
- JTAG to I2C Bridge
  - Protocol to Protocol transformation
  - IEEE 1687 or 1149.1 retargeting of I2C Host data
- System Test Message (via Ethernet stream interface)