

P2654

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Type of Project: New IEEE Standard

PAR Request Date: 14-Aug-2018

PAR Approval Date: 30-Oct-2018

PAR Expiration Date: 31-Dec-2022

Status: PAR for a New IEEE Standard

1.1 Project Number: P2654

1.2 Type of Document: Standard

1.3 Life Cycle: Full Use

2.1 Title: Standard for System Test Access Management (STAM) to Enable Use of Sub-System Test Capabilities at Higher Architectural Levels

3.1 Working Group: System Test Access Management (C/TT/STAM)

Contact Information for Working Group Chair

Name: Ian Mcintosh

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Contact Information for Working Group Vice-Chair

None

3.2 Sponsoring Society and Committee: IEEE Computer Society/Test Technology (C/TT)

Contact Information for Sponsor Chair

Name: Adam Cron

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Contact Information for Standards Representative

None

4.1 Type of Ballot: Individual

4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 04/2022

4.3 Projected Completion Date for Submittal to RevCom

Note: Usual minimum time between initial sponsor ballot and submission to Revcom is 6 months.: 10/2022

5.1 Approximate number of people expected to be actively involved in the development of this project: 30

5.2 Scope: This standard addresses use/ reuse of test assets in system context by: 1) defining a representation for behavioral descriptions of pertinent sub-assembly interfaces and of relevant data and protocol transformations; 2) defining methods for utilizing such representations to enhance management of and access to said test assets. In conjunction with existing methods for test access and test management, this will allow the coordination and control of a variety of digital interfaces to devices, boards, and sub-systems to extend test access to board and system levels. This standard does not replace or provide an alternative to existing test interface standards, but aims instead to enable their usage throughout the hierarchy of systems.

5.3 Is the completion of this standard dependent upon the completion of another standard: No

5.4 Purpose: The purpose of this standard is to facilitate a means to seamlessly integrate component access topologies, interface constraints, and other dependencies at the board and system level by using standardized descriptions focusing on topology, interfaces and behavior (as opposed to physical structure). This will ease the burden on those preparing test, maintenance and support applications, including Automatic Test Pattern Generation (ATPG), in particular where the application requires to co-ordinate control of and data transfer through multiple interfaces and/or protocols. Typically, the providers of these conforming descriptions are the producers of integrated circuits, printed circuit boards or sub-systems, including, for example, intellectual property cores in a System on Chip (SoC), with digital interfaces that are intended to be used in an automated fashion within a larger assembly. This standard will also include a methodology to ensure access to particular destination registers in the correct time order.

5.5 Need for the Project: Standards exist to access diverse feature sets for device-level test and instrumentation. However, there is currently no standard that provides for the aggregate management and coordination of such standards for higher level assemblies, such as boards or systems.

Users of board- and system-level automated test equipment need to be able to command their tools and instruments, identifying the dependencies, constraints, and required coordination. Embedded applications also need to have access to these same instruments at higher levels during run-time.

Standardization is needed to facilitate such automation and to enhance testability, test coverage, and diagnostics resolution in the higher level assemblies.

5.6 Stakeholders for the Standard: Stakeholders comprise the electronics industry at large, including, but not restricted to, designers and maintainers of electronics, particularly test developers, suppliers of test and measurement equipment and suppliers of tools for automation of electronics design and test.

Intellectual Property

6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: No

6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

7.1 Are there other standards or projects with a similar scope?: No

7.2 Joint Development

Is it the intent to develop this document jointly with another organization?: No

8.1 Additional Explanatory Notes: 1.1 Foresee this standard being the first of a family of system-test related standards and would suggest that it is assigned a number in the form "xxxx.1"