Have you ever...

… tried to use BSCAN at the system-level and found that:

- *It was hard to decide on a good scan chain architecture?*
- *The scan chain management devices caused problems with your tools?*
- *Your board-level tests needed a lot of re-work to get them running in the system?*

These are some of the issues SJTAG is working to resolve. But have you also considered how you might leverage BSCAN for other uses in your system:

- *Support hardware and software design proving by injecting faults via the scan chain?*
- *Improve detection of thermal faults in Environmental Stress Test by using short cycle time BSCAN tests?*

SJTAG is looking at "the bigger picture" for system-level applications, not just test and programming.

Get involved in SJTAG

Casually...

If you are interested in SJTAG, but don't feel you have the time to take an active part, you can still play a part.

Want to stay informed?:

- *Visit our website*
- *Sign up for our e-newsletter*
- *Get the RSS News Feeds*

Want to make a comment?:

- *Join the discussions on our Forums*
- *Review documentation on our Wiki*

Actively...

Register your interest in helping to develop a standard for system-level JTAG by contacting Ian McIntosh or by using the Contact form on our website:

http://www.sjtag.org/contact.html

The schedule for our meetings is available on the website, as are all past meeting minutes.

Chair: Ian McIntosh
E-mail: chair@sjtag.org
Web: www.sjtag.org

Copies of this brochure can be downloaded:
www.sjtag.org/index.php/documents/publications/

SJTAG_Flyer_ISO_v1.21.pub

SJTAG

The System JTAG Initiative

Scope:

This standard will develop a methodology for access to test, debug, instrument, configuration and/or programming, and emulation features (but not the features themselves) of devices via the IEEE 1149.1 Test Access Port (TAP) for the board and system (multiple board) domains.

Purpose:

The purpose of the SJTAG standard is to provide an extension of the IEEE 1149.1 standard specifically aimed at enabling the configuration, control, management, and representation of the communications required at the hierarchical system and board levels to perform operations on the IEEE 1149.1 Test Access Port (TAP) of one or more devices or device cores, in a uniform and transportable way across all system modules.

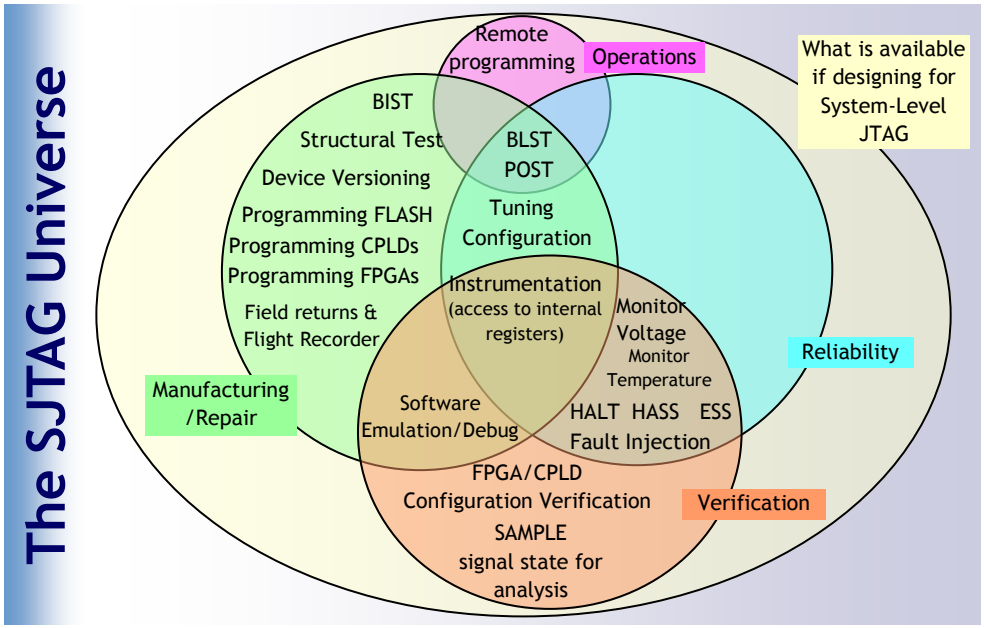
SJTAG

On the web: http://www.sjtag.org

Beyond the boundary.

SJTAG Initiative Group is:

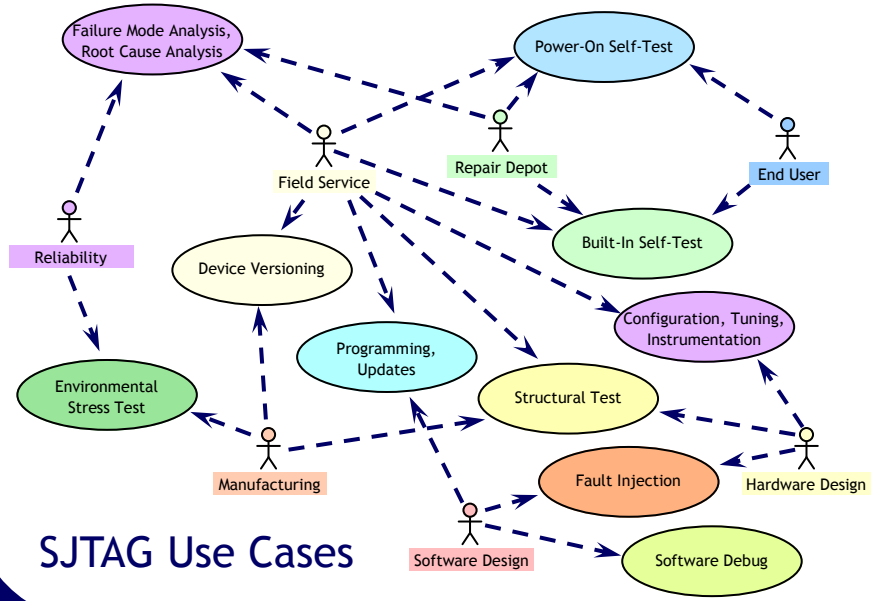
- Forerunner to the IEEE SJTAG Standard
- Analyzing and Mining common methods/ procedures/interfaces through use case analysis
- Defining partitions/interfaces in both hardware and software architectures for standardization
- Identifying minimum data sets required to support each Use Case
- Working on value propositions for each aspect of the SJTAG Universe

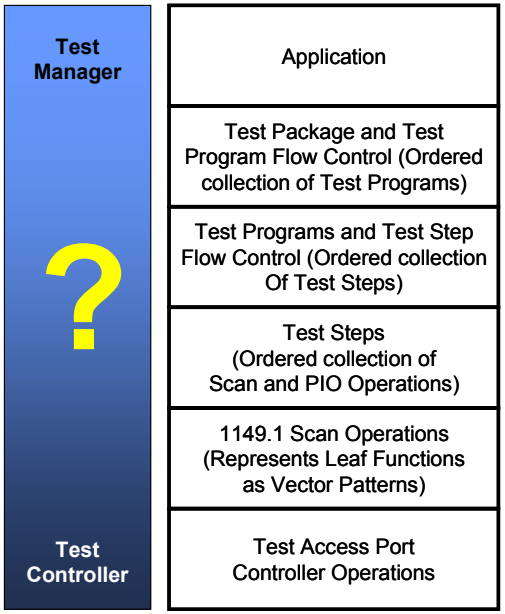


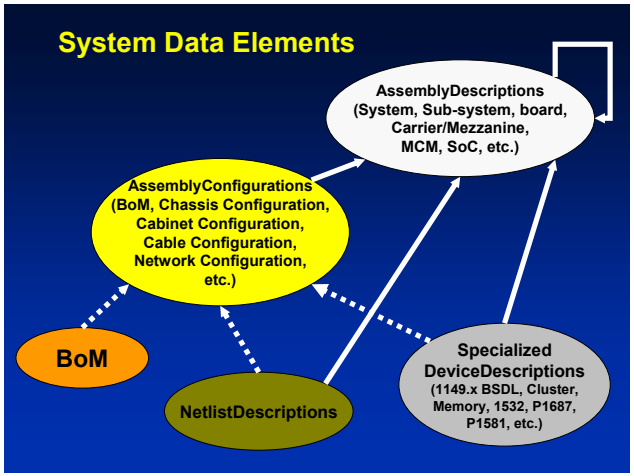
What is SJTAG?:

- SJTAG refers to the use of IEEE 1149.1 based operations with assemblies consisting of multiple boards.
- SJTAG implies hierarchical structure that leverages the board level TAPs to enable system level activities
- SJTAG extends the scope of possible uses for JTAG to applications throughout the product lifecycle
- SJTAG accommodates both external and embedded Test Controllers and Test Managers (XBST and EBST).

SJTAG Use Cases







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