Study Group Meeting #29

Ian McIntosh, Leonardo MW Ltd.

Compliance with IEEE Standards Policies and Procedures

Subclause 5.2.1 of the *IEEE-SA Standards Board Bylaws* states, "While participating in IEEE standards development activities, all participants...shall act in accordance with all applicable laws (nation-based and international), the IEEE Code of Ethics, and with IEEE Standards policies and procedures."

The contributor acknowledges and accepts that this contribution is subject to

- The IEEE Standards copyright policy as stated in the *IEEE-SA Standards Board Bylaws*, section 7, http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#7, and the *IEEE-SA Standards Board Operations Manual*, section 6.1, http://standards.ieee.org/develop/policies/opman/sect6.html

- The IEEE Standards patent policy as stated in the *IEEE-SA Standards Board Bylaws*, section 6, http://standards.ieee.org/guides/bylaws/sect6-7.html#6, and the *IEEE-SA Standards Board Operations Manual*, section 6.3, http://standards.ieee.org/develop/policies/opman/sect6.html

IEEE [TBD]
System Test Access Management
Ian McIntosh (interim chair)

Study Group Meeting #29			
Date: 2018-03-26			
Author(s):			
Name	**Affiliation**	**Phone [optional]**	**Email [optional]**
Ian McIntosh	Leonardo MW Ltd.		

Agenda

1. Roll Call

2. IEEE Patent Slides

3. Review and approve previous minutes:

4. Review open action items

5. Discussion Topics

6. Key Takeaways from today's meeting

7. Glossary terms from this meeting

8. Topic for next meeting

9. Schedule next meeting

10. Reminders

11. Any other business

12. List new action items

13. Adjourn

Instructions for the WG Chair

The IEEE-SA strongly recommends that at each WG meeting the chair or a designee:

- **Show slides #1 through #4 of this presentation**
- **Advise the WG attendees that:**
  - IEEE's patent policy is described in Clause 6 of the *IEEE-SA Standards Board Bylaws*;
  - Early identification of patent claims which may be essential for the use of standards under development is strongly encouraged;
  - There may be Essential Patent Claims of which IEEE is not aware. Additionally, neither IEEE, the WG, nor the WG Chair can ensure the accuracy or completeness of any assurance or whether any such assurance is, in fact, of a Patent Claim that is essential for the use of the standard under development.

- **Instruct the WG Secretary to record in the minutes of the relevant WG meeting:**
  - That the foregoing information was provided and that slides 1 through 4 (and this slide 0, if applicable) were shown;
  - That the chair or designee provided an opportunity for participants to identify patent claim(s)/patent application claim(s) and/or the holder of patent claim(s)/patent application claim(s) of which the participant is personally aware and that may be essential for the use of that standard
  - Any responses that were given, specifically the patent claim(s)/patent application claim(s) and/or the holder of the patent claim(s)/patent application claim(s) that were identified (if any) and by whom.

- The WG Chair shall ensure that a request is made to any identified holders of potential essential patent claim(s) to complete and submit a Letter of Assurance.
- It is recommended that the WG Chair review the guidance in *IEEE-SA Standards Board Operations Manual* 6.3.5 and in FAQs 14 and 15 on inclusion of potential Essential Patent Claims by incorporation or by reference.

  Note: **WG** includes Working Groups, Task Groups, and other standards-developing committees with a PAR approved by the IEEE-SA Standards Board.

(Optional to be shown)

◆IEEE

Participants have a duty to inform the IEEE

- Participants <u>shall</u> inform the IEEE (or cause the IEEE to be informed) of the identity of each holder of any potential Essential Patent Claims of which they are personally aware if the claims are owned or controlled by the participant or the entity the participant is from, employed by, or otherwise represents

- Participants <u>should</u> inform the IEEE (or cause the IEEE to be informed) of the identity of any other holders of potential Essential Patent Claims

Early identification of holders of potential Essential Patent Claims is encouraged

◈**IEEE**

Ways to inform IEEE

- **Cause an LOA to be submitted to the IEEE-SA (patcom@ieee.org); or**

- **Provide the chair of this group with the identity of the holder(s) of any and all such claims as soon as possible; or**

- **Speak up now and respond to this Call for Potentially Essential Patents**

If anyone in this meeting is personally aware of the holder of any patent claims that are potentially essential to implementation of the proposed standard(s) under consideration by this group and that are not already the subject of an Accepted Letter of Assurance, please respond at this time by providing relevant information to the WG Chair

Other guidelines for IEEE WG meetings

- **All IEEE-SA standards meetings shall be conducted in compliance with all applicable laws, including antitrust and competition laws.**

  - **Don't discuss the interpretation, validity, or essentiality of patents/patent claims.**

  - **Don't discuss specific license rates, terms, or conditions.**

    - Relative costs of different technical approaches that include relative costs of patent licensing terms may be discussed in standards development meetings.

      - Technical considerations remain the primary focus

  - **Don't discuss or engage in the fixing of product prices, allocation of customers, or division of sales markets.**

  - **Don't discuss the status or substance of ongoing or threatened litigation.**

  - **Don't be silent if inappropriate topics are discussed ... do formally object.**

For more details, see *IEEE-SA Standards Board Operations Manual*, clause 5.3.10 and *Antitrust and Competition Policy: What You Need to Know* at http://standards.ieee.org/develop/policies/antitrust.pdf

◆IEEE

Patent-related information

The patent policy and the procedures used to execute that policy are documented in the:

- *IEEE-SA Standards Board Bylaws*
  (http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#6)
- *IEEE-SA Standards Board Operations Manual*
  (http://standards.ieee.org/develop/policies/opman/sect6.html#6.3)

Material about the patent policy is available at
http://standards.ieee.org/about/sasb/patcom/materials.html

If you have questions, contact the IEEE-SA Standards Board Patent Committee Administrator at patcom@ieee.org

IEEE

3. Review and approve minutes

Meeting #28, March 19

Updated draft circulated March 19.

Attendees:

Ian McIntosh (Leonardo MW Ltd.) Eric Cormack (DFT Solutions Ltd.) (joined 11:32) Terry Duepner (National Instruments) Brian Erickson (JTAG Technologies) Peter Horwood (Firecron Ltd.) Bill Huynh (Marvell Inc.) Joel Irby (ARM) Mukund Modi (NAVAIR Lakehurst)	Richard Pistor (Curtiss-Wright) Naveen Srivastava (Nvidia) Jon Stewart (Dell) Brad Van Treuren (Nokia) Carl Walker (Cisco Systems) Dilipan Jayachandran (SEL, Inc.) Russell Shannon (NAVAIR Lakehurst) (joined 11:10) Louis Ungar (ATE Solutions)

4. Review open action items

Action Item Register:
http://files.sjtag.org/StudyGroup/ActionItemRegister.xls

Format of action number is
[Meeting#.Action# within that meeting]

[21.1] Supply Ian with glossary definitions used by 1687.1 for "transformation" and "retargetting".

[27.2] Legacy Initiative Group to propose definition for "SJTAG". Some contributions:
http://forums.sjtag.org/viewtopic.php?p=1308#p1308, ongoing action.

◆IEEE

5. Discussion Topics

5.a PAR - Refine PAR Scope text.

– See following slides on:

- Scope (previous draft)

  Also forum thread:
  http://forums.sjtag.org/viewtopic.php?p=1317#p1317

- Purpose (previous draft)

- Need (previous draft)

- Collation of comments around "Need"

Draft Scope

STAM Scope (19/2 proposal):

- o This standard describes methods to allow, in conjunction with existing methods, for the coordination and control of a variety of interfaces to devices, boards, and sub-systems to extend test access to the system level. The standard does not replace or provide an alternative to existing test interface standards, but aims instead to enable their usage throughout the hierarchy of the system.

From forums:
http://forums.sjtag.org/viewtopic.php?p=1316#p1316

- o This standard describes methods to allow, in conjunction with existing methods, for the coordination and control of a variety of interfaces to devices, boards, and sub-systems to extend test access to the system level. The standard does not replace or provide an alternative to existing test interface standards, but aims instead to enable their usage throughout the hierarchy of systems that adopt such methods.

Draft Purpose

STAM Purpose:

- The purpose of this standard is to provide a means to seamlessly integrate component access topologies (that follow a Capture, Shift, Update cycle), interface constraints, and other dependencies at the board and system level by using a uniform description that focuses on topology and behavior (as opposed to physical structure). By modeling this topology at the board and system level, a set of familiar and yet interchangeable interfaces may be used by higher level tools to coordinate these access topologies and provide a means of routing data sets to particular destination registers in the correct time order.

- Is this correct? If not, what do we need to change?
- Is the red text a valid constraint? Why/why not?

Draft Need

STAM Need:

- A standardized method is needed to coordinate component access topologies, interface constraints, and other dependencies at the board and system level in order to be able to effectively leverage the existing and future component level standards. Thus, a new supervisory standard is required to define the coordination and dependencies of instruments as well as configuration, management, and application of vector based testing at the board and system levels. For example, IEEE 1687 and IEEE 1149.1-2013 provide methods for describing each of the instrument interfaces on a per component basis, but do not provide the contextual prerequisites for the dependence on each instrument configuration and/or aggregation of multiple instruments for the overall board and/or system maintenance operations. Further, many components only support non-JTAG interfaces (e.g., I2C or SPI) to their instrumentation registers. This standard will provide a means to utilize the pin level access provided by other standards.

- Already know this doesn't read well; probably too wordy.

Initial collation of Need comments

- We should be looking to utilise any test features that exist within COTS items

- We need better tools, but that requires that the tools can "see" the features that are available

- Leveraging the interface standards is not the only way to do this

- (I'm just copying the following directly from Brad's post as I couldn't see a better way of incorporating it here)
    - *SJTAG is intended to improve the ability to test, diagnose and provide prognostic health information about systems.*
        - *(Analyze from top down in decomposition is necessary to be able to know what has to be exposed. How someone implements it is less important if it is clearly documented and usable. Testablilty "flow down" may be outside of SJTAG scope : Testability Framework Requirements. Available Testability "flow up" is what is advertised from the bottom up: Availability of Testability Features.)*
    - A standardized method is needed to coordinate
        - *(coordinate - exposure of underlying test capabilities that might exist?) (everyone puts testability at their level and don't usually plan for use at a higher level) (Documentation of what is available at each level is key.)*
    - ~~component~~
        - *(component could relate to discretes and not what we want)*
    - access topologies,
        - *(Board level BIST is more than a component access topology.)*
    - interface constraints, and other dependencies at the board and system level
        - *(Should really focus on system and sub-systems, which includes boards.)*
    - in order to be able to effectively leverage the existing and future component level standards. Thus, a new supervisory standard is required to define the coordination and dependencies of instruments as well as configuration, management, and application of vector based testing at the board and system levels.
        - *(The higher up you go in the hierarchy, the more you morph into functional testing.) (Downloading code into modules and executing them is also part of this infrastructure that is needed.)*

- Specific interfaces are not really broad enough for the Needs statement

- This standard recognizes the need for some form of standardized measurement of test coverage and quality of test, but this standardization effort does not attempt to address that need (Additional comment: As this, or words to this effect, describe an *exclusion* from the standard, it *could* become part of the stated Scope instead of the Need)

- Should be inclusive of diverse Use Cases (and not preclude any), but should they be detailed in the PAR?

Wrap-up items

6. Today's Key Takeaways

7. Glossary terms from this meeting

8. Topic for next meeting

9. Schedule next meeting
   April 2, 2018 is Easter Monday. April 9?

10. Reminders
    Think about potential officers, moving towards a Working Group.

11. Any other business

12. List new action items

13. Adjourn