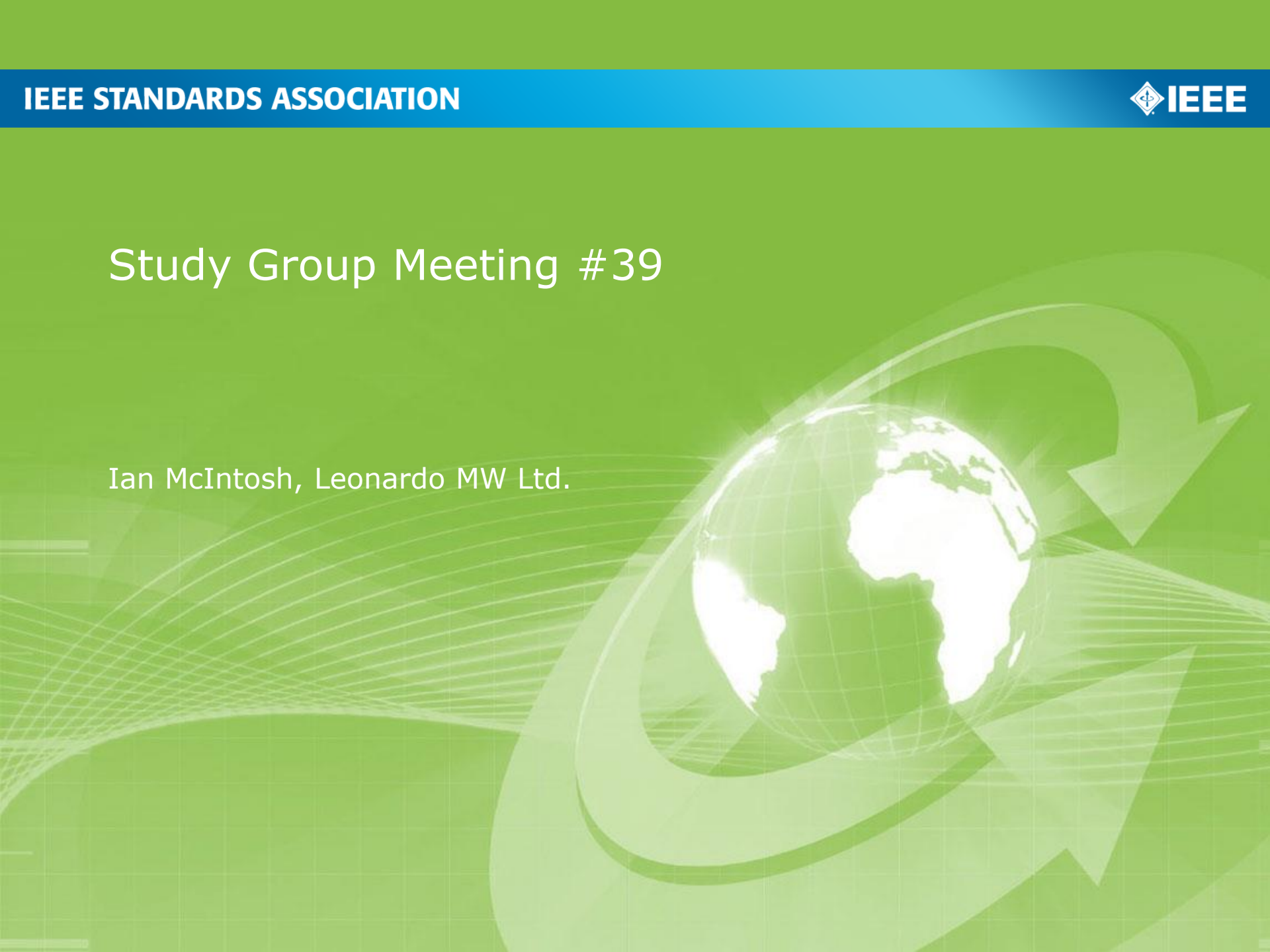
Study Group Meeting #39

Ian McIntosh, Leonardo MW Ltd.



Compliance with IEEE Standards Policies and Procedures

Subclause 5.2.1 of the *IEEE-SA Standards Board Bylaws* states, "While participating in IEEE standards development activities, all participants…shall act in accordance with all applicable laws (nation-based and international), the IEEE Code of Ethics, and with IEEE Standards policies and procedures."

The contributor acknowledges and accepts that this contribution is subject to

- The IEEE Standards copyright policy as stated in the *IEEE-SA Standards Board Bylaws*, section 7, http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#7, and the *IEEE-SA Standards Board Operations Manual*, section 6.1, http://standards.ieee.org/develop/policies/opman/sect6.html
- The IEEE Standards patent policy as stated in the *IEEE-SA Standards Board Bylaws*, section 6, http://standards.ieee.org/guides/bylaws/sect6-7.html#6, and the *IEEE-SA Standards Board Operations Manual*, section 6.3, http://standards.ieee.org/develop/policies/opman/sect6.html

IEEE [TBD]
System Test Access Management
Ian McIntosh (interim chair)

Study Group Meeting #39			
Date: 2018-06-18			
Author(s):			
Name	**Affiliation**	**Phone [optional]**	**Email [optional]**
Ian McIntosh	Leonardo MW Ltd.		

Agenda

1. Roll Call
2. IEEE Patent Slides
3. Review and approve previous minutes:
4. Review open action items
5. Discussion Topics:
   - Voting results, Update on “Stakeholders”; Proposed amendments
6. Key Takeaways from today's meeting
7. Glossary terms from this meeting
8. Topic for next meeting
9. Schedule next meeting
10. Reminders
11. Any other business
12. List new action items
13. Adjourn

Instructions for the WG Chair

The IEEE-SA strongly recommends that at each WG meeting the chair or a designee:

- **Show slides #1 through #4 of this presentation**
- **Advise the WG attendees that:**
  - IEEE's patent policy is described in Clause 6 of the *IEEE-SA Standards Board Bylaws*;
  - Early identification of patent claims which may be essential for the use of standards under development is strongly encouraged;
  - There may be Essential Patent Claims of which IEEE is not aware. Additionally, neither IEEE, the WG, nor the WG Chair can ensure the accuracy or completeness of any assurance or whether any such assurance is, in fact, of a Patent Claim that is essential for the use of the standard under development.
- **Instruct the WG Secretary to record in the minutes of the relevant WG meeting:**
  - That the foregoing information was provided and that slides 1 through 4 (and this slide 0, if applicable) were shown;
  - That the chair or designee provided an opportunity for participants to identify patent claim(s)/patent application claim(s) and/or the holder of patent claim(s)/patent application claim(s) of which the participant is personally aware and that may be essential for the use of that standard
  - Any responses that were given, specifically the patent claim(s)/patent application claim(s) and/or the holder of the patent claim(s)/patent application claim(s) that were identified (if any) and by whom.
- The WG Chair shall ensure that a request is made to any identified holders of potential essential patent claim(s) to complete and submit a Letter of Assurance.
- It is recommended that the WG Chair review the guidance in *IEEE-SA Standards Board Operations Manual* 6.3.5 and in FAQs 14 and 15 on inclusion of potential Essential Patent Claims by incorporation or by reference.

Note: **WG** includes Working Groups, Task Groups, and other standards-developing committees with a PAR approved by the IEEE-SA Standards Board.

02 January 2018

(Optional to be shown)

Participants have a duty to inform the IEEE

- Participants shall inform the IEEE (or cause the IEEE to be informed) of the identity of each holder of any potential Essential Patent Claims of which they are personally aware if the claims are owned or controlled by the participant or the entity the participant is from, employed by, or otherwise represents

- Participants should inform the IEEE (or cause the IEEE to be informed) of the identity of any other holders of potential Essential Patent Claims

Early identification of holders of potential Essential Patent Claims is encouraged

Ways to inform IEEE

- **Cause an LOA to be submitted to the IEEE-SA (patcom@ieee.org); or**
- **Provide the chair of this group with the identity of the holder(s) of any and all such claims as soon as possible; or**
- **Speak up now and respond to this Call for Potentially Essential Patents**

If anyone in this meeting is personally aware of the holder of any patent claims that are potentially essential to implementation of the proposed standard(s) under consideration by this group and that are not already the subject of an Accepted Letter of Assurance, please respond at this time by providing relevant information to the WG Chair

Other guidelines for IEEE WG meetings

- All IEEE-SA standards meetings shall be conducted in compliance with all applicable laws, including antitrust and competition laws.
  - Don't discuss the interpretation, validity, or essentiality of patents/patent claims.
  - Don't discuss specific license rates, terms, or conditions.
    - Relative costs of different technical approaches that include relative costs of patent licensing terms may be discussed in standards development meetings.
      - Technical considerations remain the primary focus
  - Don't discuss or engage in the fixing of product prices, allocation of customers, or division of sales markets.
  - Don't discuss the status or substance of ongoing or threatened litigation.
  - Don't be silent if inappropriate topics are discussed … do formally object.

For more details, see *IEEE-SA Standards Board Operations Manual*, clause 5.3.10 and *Antitrust and Competition Policy: What You Need to Know* at http://standards.ieee.org/develop/policies/antitrust.pdf

Patent-related information

The patent policy and the procedures used to execute that policy are documented in the:

- *IEEE-SA Standards Board Bylaws*
  (http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#6)
- *IEEE-SA Standards Board Operations Manual*
  (http://standards.ieee.org/develop/policies/opman/sect6.html#6.3)

Material about the patent policy is available at
http://standards.ieee.org/about/sasb/patcom/materials.html

If you have questions, contact the IEEE-SA Standards Board Patent Committee Administrator at patcom@ieee.org

3. Review and approve minutes

Meeting #38, June 11

Updated draft circulated June 11.

Attendees:

Ian McIntosh (Leonardo MW Ltd.) Eric Cormack (DFT Solutions) Bill Eklow (Retired) Brian Erickson (JTAG Technologies) Peter Horwood (Firecron Ltd.) (joined 11:30) Bill Huynh (Marvell Inc.)	Jon Stewart (Dell) Brad Van Treuren (Nokia) Carl Walker (Cisco Systems) Russell Shannon (NAVAIR Lakehurst) Louis Ungar (ATE Solutions) Sivakumar Vijayakumar (Keysight)

4. Review open action items

Action Item Register:
http://files.sjtag.org/StudyGroup/ActionItemRegister.xls

Format of action number is
[Meeting#.Action# within that meeting]

[21.1] Supply Ian with glossary definitions used by 1687.1 for "transformation" and "retargetting".

[27.2] Legacy Initiative Group to propose definition for "SJTAG". No recent contributions: http://forums.sjtag.org/viewtopic.php?p=1314#p1314, ongoing action.

5. Discussion Topics

5.a Voting results. Eligible 12, M1: 12 for votes. M2 11 for votes, 1 abstention. M3 12 for votes. Motions carried.

5.b Update on "Stakeholders".

- Format doesn't really matter; Adam Cron preferred the list of roles ("by technology" in last week's notes).
- Suggestion:
  "The electronics industry at large including, but not restricted to, …" then pick 3-5 from last week's list that seem to be key.

5.c Proposed Amendments

- Refer to marked up document from Adam Ley:
  http://files.sjtag.org/StudyGroup/2018_06_11_PAR_texts_annotated.docx

Stakeholders

The electronics industry at large including, but not restricted to, Test Developers, Designers and Maintainers of Electronics, Test and Measurement Equipment Manufacturers, Electronic Design Automation Tool Suppliers, Test Tool Suppliers.

P1838 lists “The semiconductor industry at large, including Integrated Device Manufacturers (IDMs), foundries, fab-light and fab-less semiconductor companies, design houses, Intellectual Property (IP) core providers, vendors of Electronic Design Automation (EDA) tools, OutSourced Assembly & Test (OSAT) houses, companies in the IC test industry, board and system manufacturers.”

P1687.2 and P2427 each list “Integrated-circuit (IC) designers, IC test engineers, IC suppliers, IC users.”

Wrap-up items

6. Today's Key Takeaways
7. Glossary terms from this meeting
8. Topic for next meeting
9. Schedule next meeting
   June 25
10. Reminders
    We need to submit our Draft PAR to TTSC by the end of June.
    Think about potential officers, moving towards a Working Group.
11. Any other business
12. List new action items
13. Adjourn

Motion 1: Brad Van Treuren moves that the group adopts the text of the Scope, as revised at the June 11 meeting, for the STAM PAR, seconded by Eric Cormack.

Motion 2: Bill Eklow moves that the group adopts the text of the Purpose, as revised at the June 11 meeting, for the STAM PAR, seconded by Brad Van Treuren.

Motion 3: Louis Ungar moves that the group adopts the text of the Need, as written at the June 4 meeting, for the STAM PAR, seconded by Jon Stewart.

STAM Scope: This standard: 1) defines a representation of conforming behavioral descriptions of interfaces and transformations, 2) defines methods for utilizing those representations to enhance the test management and access to sub-assembly test assets. In conjunction with existing methods, this will allow the coordination and control of a variety of digital interfaces to devices, boards, and sub-systems to extend test access to board and system levels. The standard does not replace or provide an alternative to existing test interface standards, but aims instead to enable their usage throughout the hierarchy of systems.

STAM Purpose: The purpose of this standard is to provide a means to seamlessly integrate component access topologies, interface constraints, and other dependencies at the board and system level by using standardized descriptions focusing on topology, interfaces and behavior (as opposed to physical structure). This will ease the burden on those preparing test, maintenance and support applications, including Automatic Test Pattern Generators (ATPGs), in particular where the application requires to co-ordinate control of and data transfer through multiple interfaces and/or protocols. Typically, the providers of these conforming descriptions are the producers of assemblies of integrated circuits, printed circuit boards or sub-systems, including, for example, intellectual property cores in a System on Chip (SoC), with digital interfaces that are intended to be used in an automated fashion within a larger assembly. This standard will also include a methodology to ensure access to particular destination registers in the correct time order.

STAM Need: Standards exist to access diverse feature sets for device level test and instrumentation. However, there is currently no standard that provides for the aggregate management and coordination of such standards for higher level assemblies, such as boards or systems.

Users of board and system level automated test equipment need to be able to command their tools and instruments, identifying the dependencies, constraints, and required coordination. Embedded applications also need to have access to these same instruments at higher levels during run-time.

Standardization is needed to facilitate such automation and to enhance testability, test coverage, and diagnostics resolution in the higher level assemblies.